iSTART

Technical white paper of the highly configurable RRAM IP testing and repairing circuits development environment: EZ-NBIST

iSTART

1. Testing methodologies of RRAM IP

The testing methodologies of RRAM IP covers full wafer sort, and final test for UMC's 22nm process and customized embedded RRAM IP.

iSTART-TEK develops EZ-NBIST GUI tool to save BIST coding time of RRAM IP.

EZ-NBIST follows RRAM vendor's testing methodologies to implement all test items' timing diagrams and save parallel long testing time in ATE.

2. Why RRAM IP needs to use BIST and BISR?

RRAM IP has complicated testing functions to cover each disturbing condition in 22nm process.

The memory BIST adds logic to an IC which allows the SoC to test its own memory operation.

MBIST tests the RRAM macro through an effective test algorithm to detect possibly all the faults. MBIST generates test patterns from RRAM vendor requirement to the RRAM macro and reads them to find any RRAM defects.

BISR adds repair circuit to backup memory to increase the RRAM IC yield.

3. How iSTART-TEK accomplish BIST and BISR of RRAM IP?

iSTART-TEK develops EZ-NBIST GUI tool to generate BIST and BISR of RRAM IP.

iSTART-TEK BIST implements all RRAM test items to cover wafer soft and final test. BIST interface is a flexible serial interface to reduce IC test pins. Increase BIST test flexibility, all test items can be enabled and disabled individually. Provide diagnosis mode to debug defect address.

iSTART-TEK BISR records RRAM faulty memory address and use redundancy to increase RRAM IC yield. Provide auto repair function.

Figure 1 shows RRAM test and repair solutions.

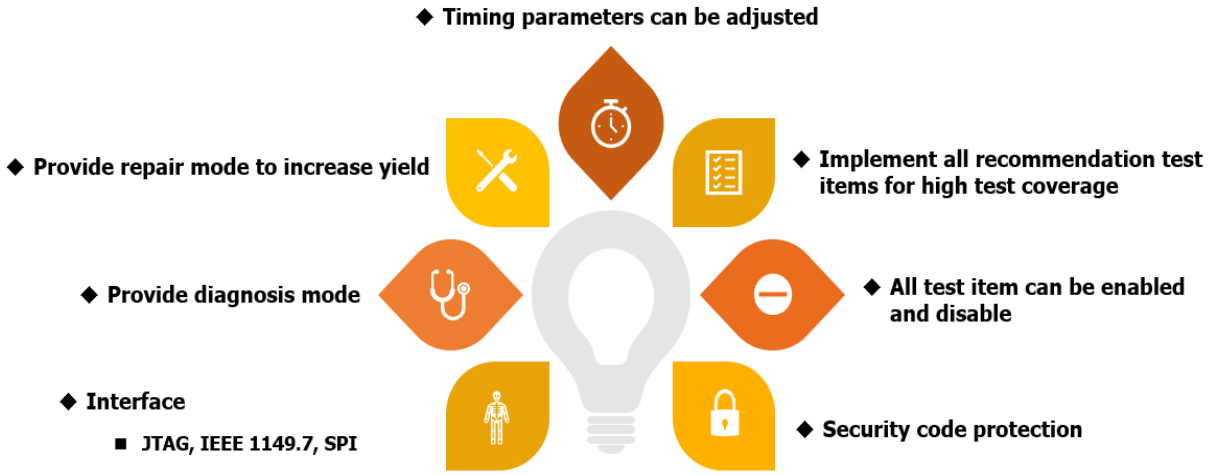

Figure 1

Figure 2 shows RRAM test and repair features.

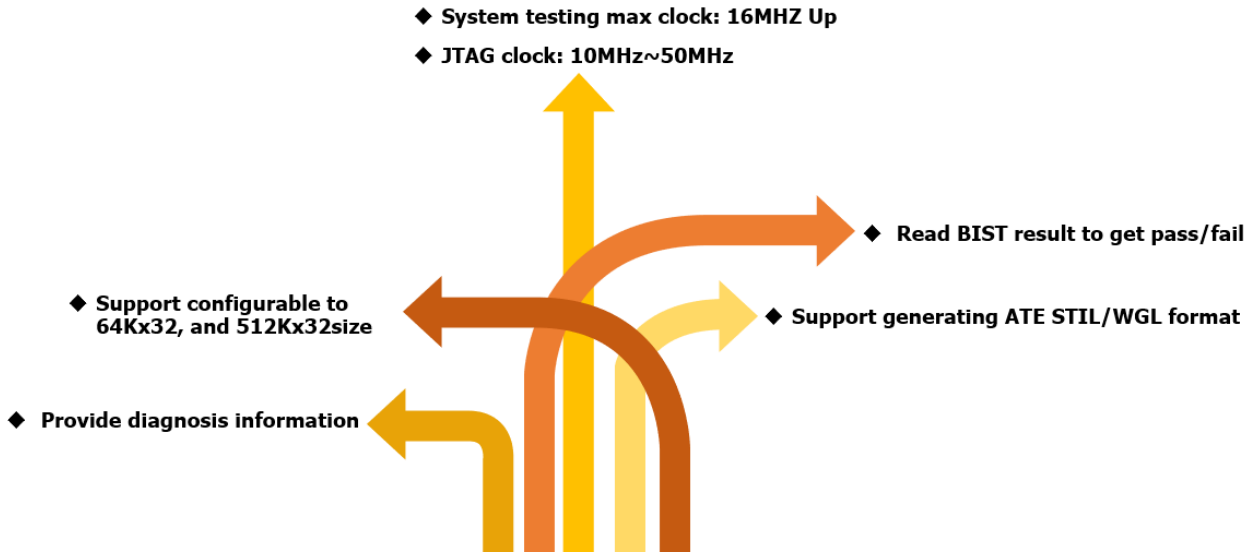

Figure 2

Figure 3 shows RRAM diagnosis simulation output.

```
item cnt: 374
addr:     1
fault_bit:00000000000000000000010000000000

item cnt: 374
addr:   255
fault_bit:00000000000000000000010000000000

item cnt: 374
addr:   511
fault_bit:00000000000000000000010000000000

item cnt: 374
addr:   521
fault_bit:00000000000000000000010000000000

item cnt: 374
addr:   541
fault_bit:00000000000000000000010000000000
```

Figure 3

Figure 4 shows BISR circuit block.

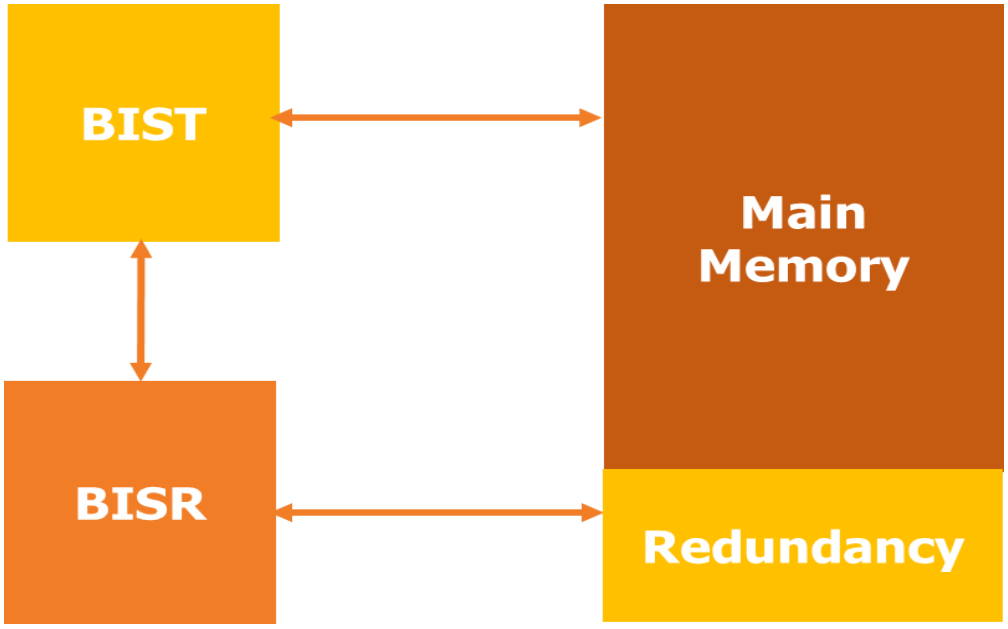

Figure 4

4. What is EZ-NBIST?

EZ-NBIST is an RRAM GUI tool to generate BIST and BISR of RRAM IP.

錯誤! 找不到參照來源。 shows the perspective of EZ-NBIST GUI. Click "EZ-NBIST Config" from "Config"

drop-down menu.

Figure 5

Users click "Run…" from "Run" drop-down menu to execute EZ-NBIST in Figure 6.

Figure 6

5. How many RRAM IP are included in EZ-NBIST?

EZ-NBIST GUI supports following RRAM IP for UMC 512Kx32, 64Kx32 IP sizes and customized IP sizes.

Users can choose customized RRAM macro types, vendor types and specific RRAM macro sizes as shown in Figure 7 and Figure 8.

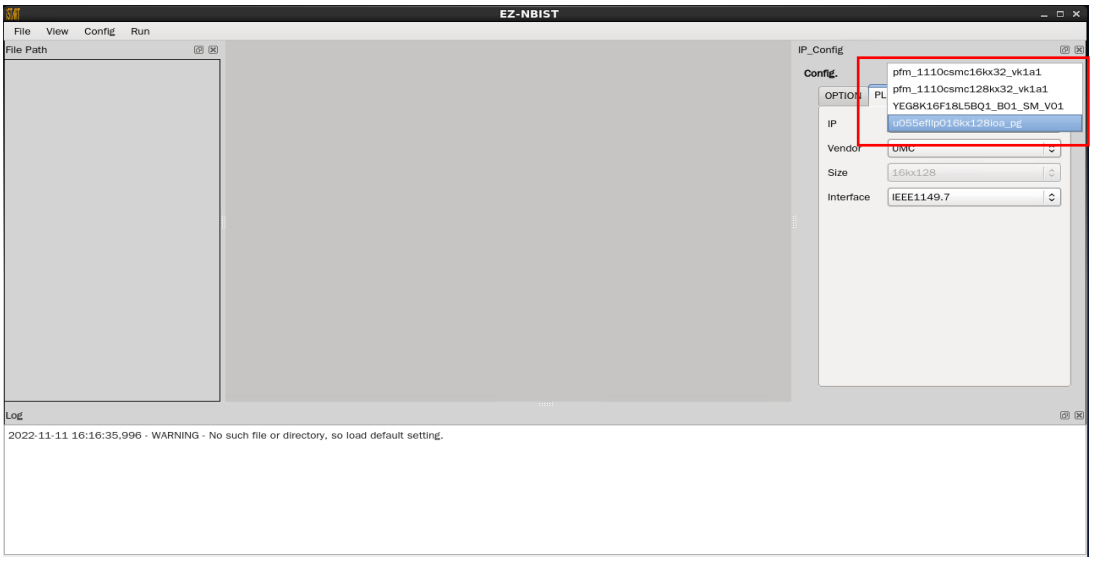

Figure 7

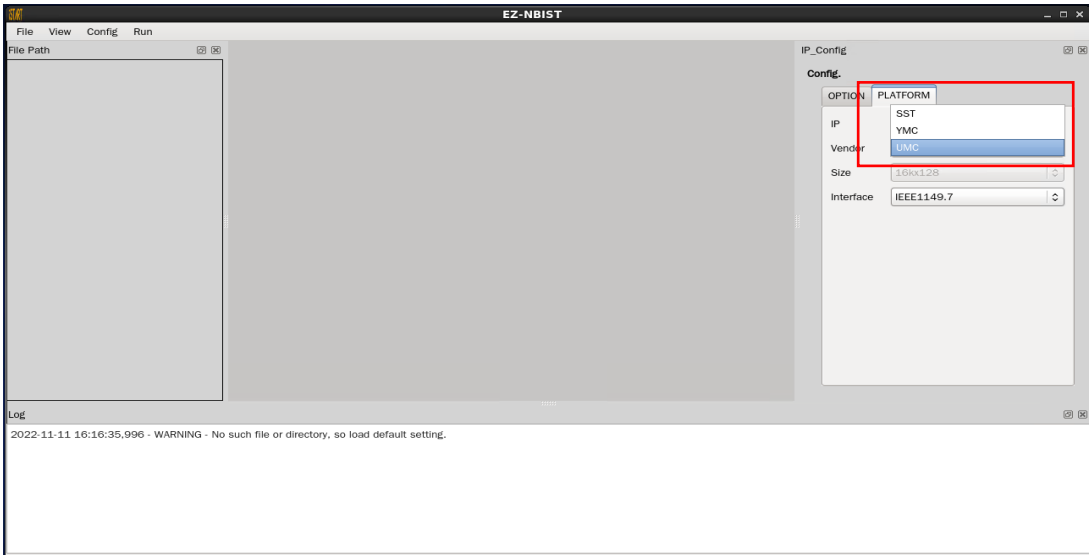

Figure 8

6. What kinds of interface are included in EZ-NBIST?

EZ-NBIST GUI supports 3 flexible serial interfaces JTAG, IEEE1149.7, and SPI as shown in Figure 9.

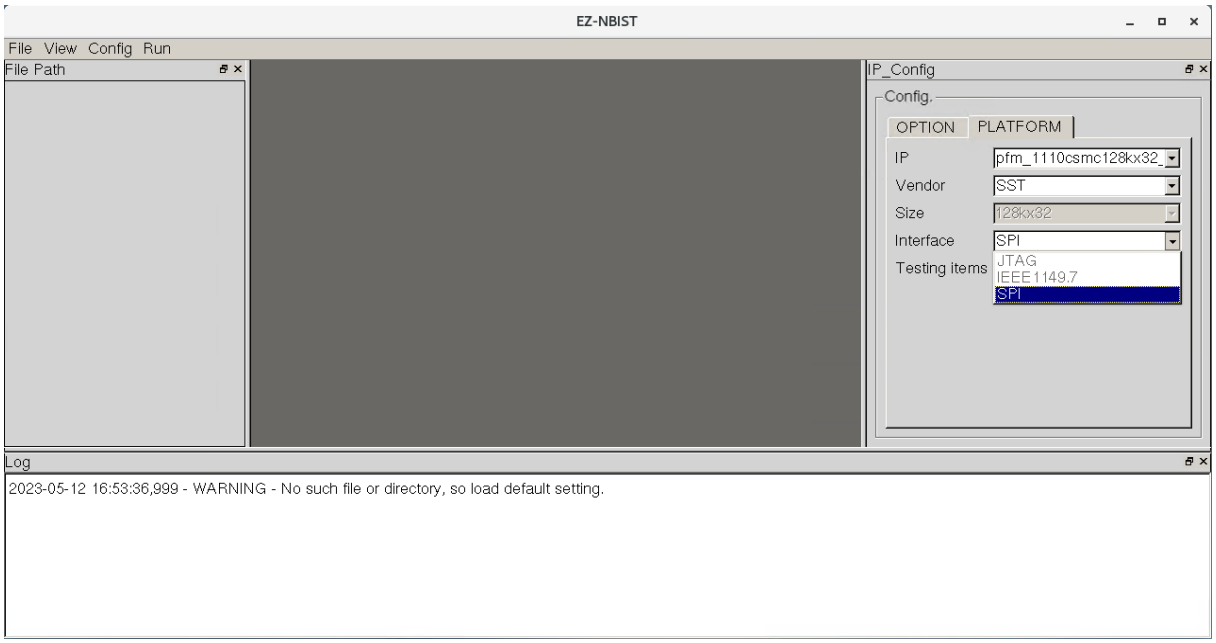

Figure 9

Figure 10 shows RRAM test and repair block with IEEE1149.7 interface.

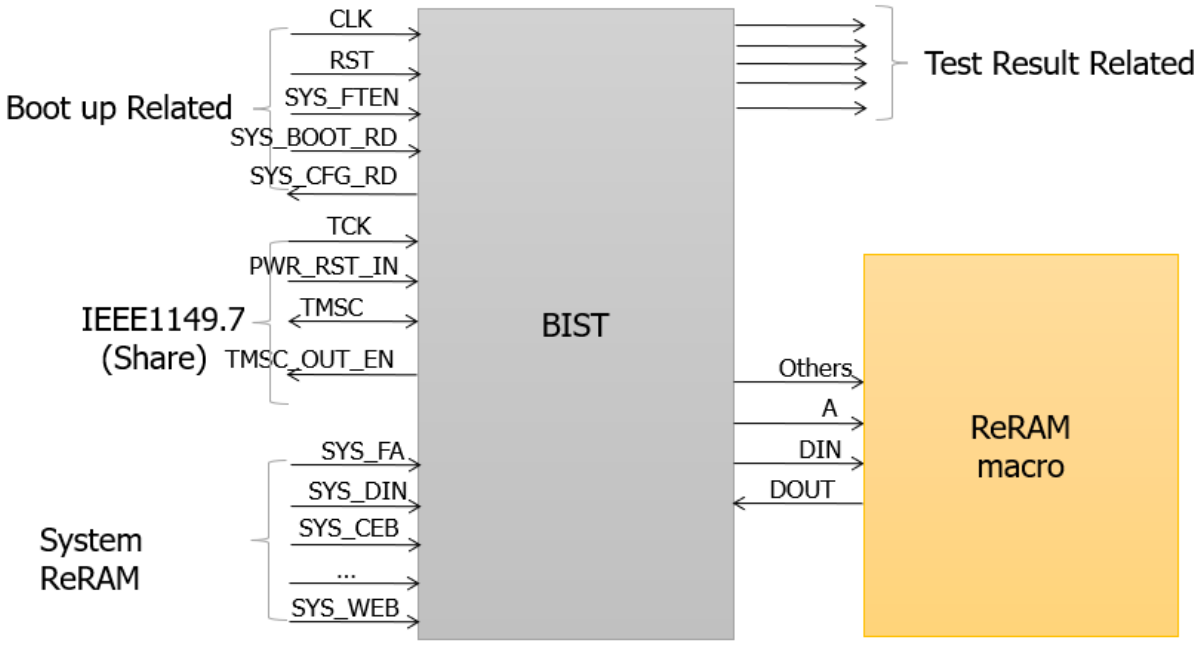

Figure 10

7. How flexibility of EZ-NBIST?

EZ-NBIST supports configurable BIST and BISR IP for different RRAM macro sizes. All RRAM timing parameters can be adjusted. Figure 11 shows all test items can be enabled and disabled individually.

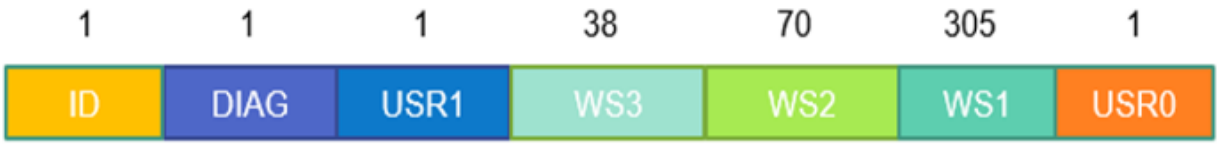

Figure 11

EZ-NBIST can help users to generate the complete synthesis RTL, the verification environment, the testing patterns, the behavior model, and the customized RRAM database as shown in Figure 12.

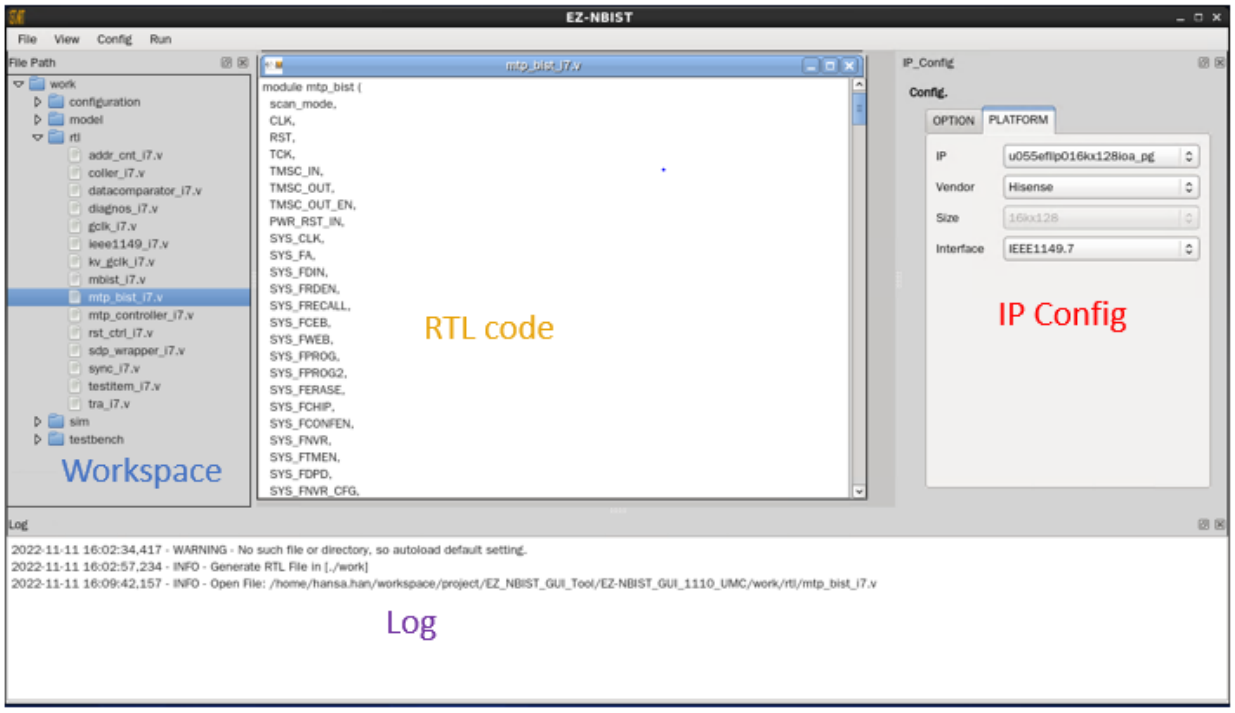

Figure 12

To execute simulation with RRAM model, users can select a test pattern to generate simulation dump files. For example, execute "2" in
Figure 1 to start "ws1" testing item's simulation flow.

Figure 13

8.Conclusion

EZ-NBIST provides RRAM BIST/BISR with professional testing items. EZ-NBIST saves RRAM tuning parameter timing time in ATE. The RRAM BIST and BISR area overhead of SoC is acceptable.
EZ-NBIST is also easy to set for accomplishing RRAM IP's testing circuit.