iSTART

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# iSTART iReport

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# iSTART-TEK has Successfully Obtained the Chinese Patent for "Memory Repair Circuit, Memory Module, and Memory Repair Method"

iSTART-TEK has successfully obtained the Chinese patent for "Memory Repair Circuit, Memory Module, and Memory Repair Method" (Patent No: ZL 2019 1 1227376.5).

This patent addresses the limitations of existing hardware and software repair techniques by enhancing repair efficiency, reducing time costs, and ensuring the proper functioning of electronic products. It includes components such as non-volatile and volatile memory units, controllers, self-test circuits, and repair information generation circuits.

The patented technology combines the advantages of both hardware and software repair methods, offering incremental repair capabilities. In applications requiring long-term use of electronic devices, this memory repair circuit and the associated memory module can fix newly emerged faulty memory units, overcoming the limitations of current repair techniques.

# The Rise of AI Applications: iSTART-TEK's Memory Testing and Repair Technology Boosts Yield

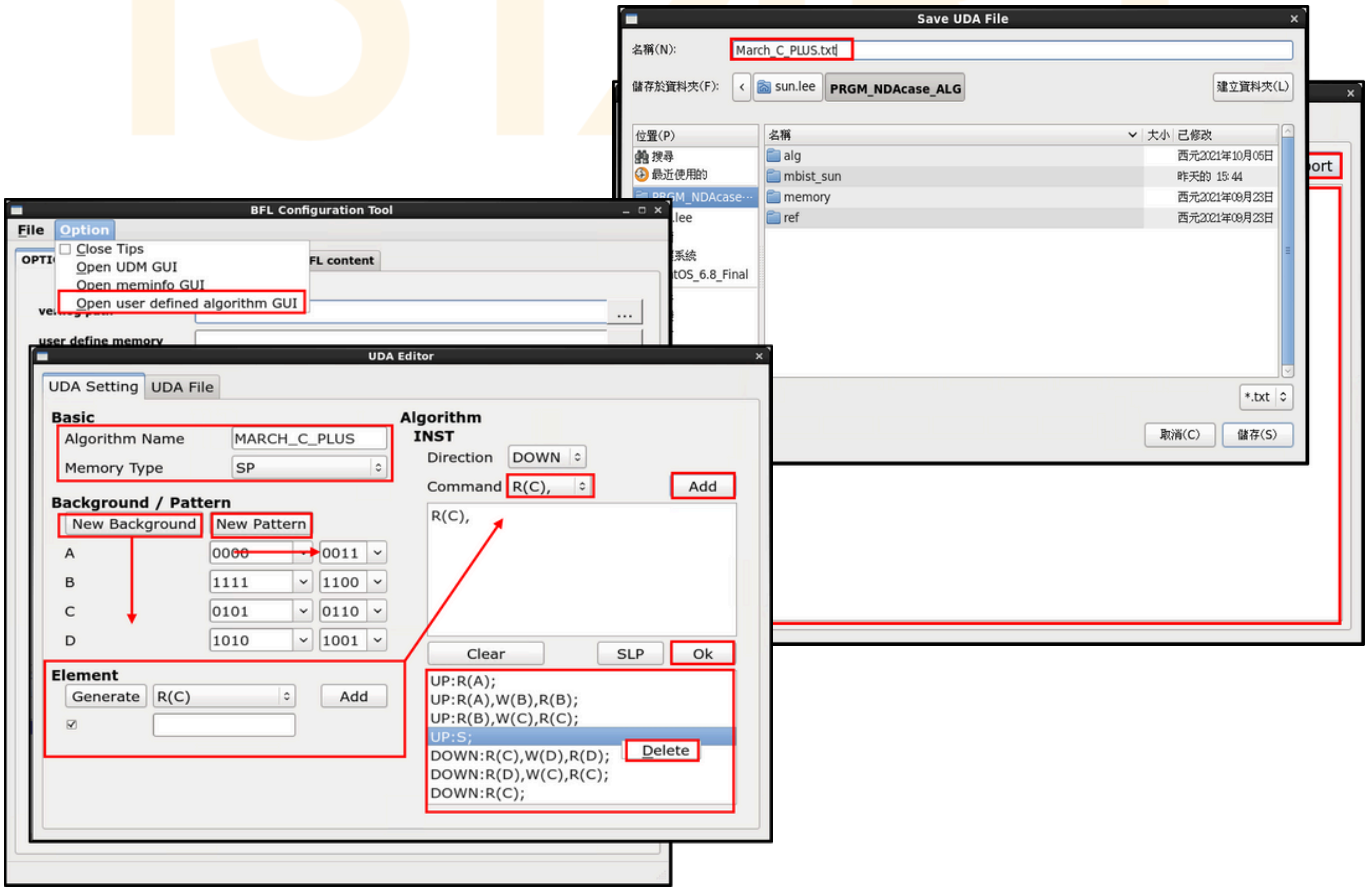
Memory has been in use for over 50 years, and the development and application of semiconductors in the past were not as advanced and diverse as they are today. From earlier PC and laptop products to the applications in mobile phones and mining machines, and now to the trending electric vehicles and AI in 2024, these advancements are driving semiconductors toward new applications.

AI applications require powerful computational capabilities, significantly increasing the proportion of memory within System on Chips (SoC). Traditional March C algorithms can no longer meet the yield requirements of various wafer manufacturers. If algorithms cannot effectively identify memory defects, it will be impossible to repair the chips to a usable state. To fulfill customers' needs for rigorous and flexible memory testing, and effectively control DPPM (Defective Parts Per Million), iSTART-TEK has developed UDA (User-Defined Algorithm) and EZ-TEC IP to offer customers the optimal testing solutions.

# Press Release

UDA can meet customers' demands for flexible and user-defined testing algorithms. Design engineers can use GUI (Graphical User Interface) to quickly generate memory testing algorithms. CIM (Computing in Memory) needs to compute directly in memory instead of through the CPU (Central Processing Unit).

In existing testing algorithms, the input and output patterns are identical, meaning that the written data and read data are the same. This allows for comparison of memory data to ensure correctness. Thus, for CIM memory, it is necessary to generate and compare input and output data with different patterns to verify if the CIM memory is functioning correctly.

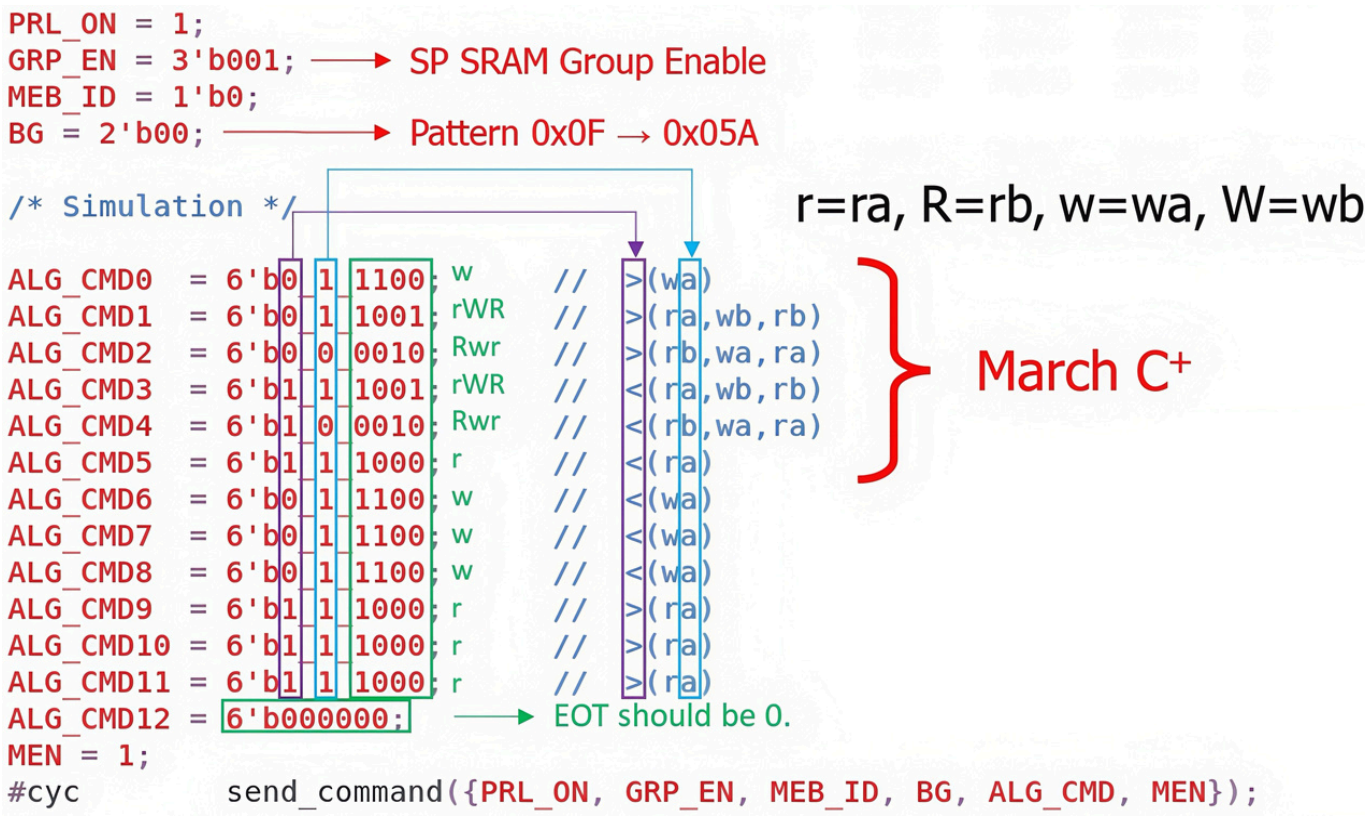



Easy to Choose Algorithms in GUI of UDA

EZ-TEC IP is a modularized architecture SRAM IP developed based on iSTART-TEK's patent, “METHOD FOR GENERATING A MEMORY BUILT-IN SELF-TEST ALGORITHM CIRCUIT”. Currently, common memory testing algorithms in the market often involve redundant testing, leading to increased testing time and costs. Moreover, as advanced processes continue to progress, existing testing algorithms may fail to detect memory defects in these advanced processes and cannot meet the evolving demands.

EZ-TEC IP is an advanced technology that effectively addresses this issue by providing test engineers with flexible reconfiguration of testing algorithms.

In existing testing algorithms, the execution sequence is fixed once the chip design is completed, making dynamic adjustments impossible during the mass production testing phase. However, EZ-TEC IP allows test engineers to adjust the sequence of test elements, such as W, rWR, and Rwr, during the mass production testing phase according to their needs. Additionally, it is possible to increase or decrease the number of times elements are executed, thereby enhancing the intensity of memory testing. This products and prevents substandard wafers from reaching customers.




Arrangements of Elements

The UDA combined with EZ-TEC IP can be integrated into a standalone IP, which does not interfere with the customer's existing DFT solutions. Additionally, it incorporates iSTART-TEK's solutions, resulting in only a slight increase in the customer's cost while significantly enhancing chip testing quality.

When incorporating iSTART-TEK's repair technology, it can further improve the overall chip yield and more effectively reduce DPPM, ensuring the highest quality for the customers' chips.

# iSTART-TEK's Memory Repair Technology Becomes a Key Player in the AI Era

The advancements in Artificial Intelligence (AI) technology have endowed AI systems with the ability to perceive, learn, reason, analyze, communicate, understand, and solve problems. As semiconductor technology continues to evolve, chip design and functionality have progressed from simple arithmetic logic operations to now incorporating AI capabilities. However, developing AI chips involves rigorous verification processes to ensure stable operation. For instance, Blackwell, a well-known company's AI chip, faced shipment delays due to design defects.

This not only impacted the company's expected $200 billion revenue in 2025 but also caused significant losses in the product development timelines and reputations of its customers. Therefore, ensuring that large-scale chips meet functional requirements and maintain high yield rates has become a top priority for chip designers during product development.

High-quality chips require not only powerful functionality but also comprehensive testing and validation solutions to ensure high yield.

Especially in the AI chip field, to meet complex computing demands, various types of memory are embedded in the chips, with memory sometimes occupying more than 60% of more than 60% of the total chip area. Thus, memory yield is one of the critical factors in determining whether an AI chip can function properly. To ensure that memory functions correctly, testing solutions like MBIST (Memory Built-in Self-Test) are widely used. When memory errors are detected, MBISR (Memory Built-in Self Repair) is employed to correct them, improving overall yield.

As one of the few EDA tool and IP providers in the industry offering MBIST/MBISR testing solutions, iSTART-TEK has gained the favor of internationally renowned companies through its patented architecture and highly efficient memory repair technology.

**Memory Repair Technology Features**

- Simplified operation interface: iSTART-TEK's memory repair technology has surpassed the limitations of traditional template-based design by adopting an innovative Turn-on & Generation approach. This allows customers to easily complete circuit repair and significantly shorten the development cycle.

- High-performance technology: iSTART-TEK offers both Soft Repair and Hard Repair solutions, providing customers with flexible options based on chip performance efficiency or cost requirements.
- Redundancy repair technology: When redundant memory cannot be generated, iSTART-TEK's "Stand-alone" repair technology can be utilized to achieve self-repair functionality for the memory.
- EZ-Safety IP is an independent IP that can notify and initiate memory testing in real-time during chip operation. If any defects are detected during testing, EZ-Safety IP can also perform repairs, ensuring the chip continues to function stably.

These memory repair technologies offer chip designers flexible options and can be applied across various IC designs, particularly in mainstream AI chip development. As the importance of AI applications escalates worldwide, leveraging professional and mature EDA tools becomes essential to achieving satisfactory yields in AI chip production.

# Balance Chip Costs and Quality

The book Chip War clearly illustrates the entire history of the semiconductor industry, from Gordon Moore's introduction of Moore's Law and Robert Noyce's founding of Intel to Morris Chang's establishment of TSMC.

The semiconductor industry has always been a battleground for top players, where even a single misstep can lead to the loss of market position or even ruthless elimination. For example, both South Korea's Samsung and CPU giant Intel have faced strategic missteps and manufacturing bottlenecks, causing their technology and market share to lag far behind TSMC.

Elon Musk, CEO of Tesla, has utilized a well-known concept called the "Idiot Index" to measure how much more the cost of a finished product is compared to the cost of its basic components. If this index is too high, it indicates that the component design is too complex or inefficient and requires more advanced manufacturing techniques to reduce costs. In the chip industry, companies employ various strategies to cut costs, such as self-development or reducing non-essential auxiliary designs.

However, self-development carries risks. Companies may lack experience or fail to design products that meet market demands, which can ultimately lead to failure and the loss of market opportunities.

Newton once said, “If I have seen further, it is by standing on the shoulders of giants.” The reason why the chip industry can rapidly develop following Moore's Law is that those “shoulders of giants” can always be replicated. Chip design companies often purchase mature IP to quickly launch the products that meet the market demands, and integrate these IPs into their technology and products to accelerate the new product design process.

In today's chip design industry, the most pressing issue is how to prevent end users from receiving defective chips while ensuring high quality, all while considering design costs. This balance often becomes a critical factor in determining whether a chip design company can survive in the competitive market.

iSTART-TEK specializes in Memory Built-In Self-Test (MBIST) and memory Built-In Self-Repair (MBISR) technologies for many years, providing high-quality self-diagnostic circuits for customers. Through these solutions, iSTART-TEK has helped customers repair over 50% of defective chips, significantly improving product yield rates. iSTART-TEK is also the only enterprise in Greater China that have achieved ISO 26262 TCL1 certification, the highest level of software tool confidence certification.

iSTART-TEK's EDA tools include START and EZ-BIST, while its IP offerings include eFlash BIST IP, EZ-TEC IP, EZ-Safety IP, and EZ-Monitor IP. The company's patented customized functions, such as highly efficient memory repair technology-recognized by a Chinese patent-and User-Defined Algorithm (UDA), which have been granted a U.S. patent, enable customers to swiftly complete the necessary testing designs for modern chips. These patented functions ensure high-quality chips with minimal impact on circuit size, with the added circuitry occupying less than 1.5% of the total memory area.

As a result, iSTART-TEK's memory testing and repair solutions provide chip designers with an optimal balance between chip quality and cost efficiency.

iSTART-TEK is committed to delivering highly cost-effective products, helping customers significantly reduce development time and costs. With its competitive pricing and high-quality offerings, iSTART-TEK has become the preferred choice for numerous chip design companies.

# iSTART-TEK's eFlash Testing and Repair IP are Widely applied in Automotive Electronic Chips

The global automotive industry is moving toward electrification and smart technology development. As automotive electronics technology continues to advance, the demand for automotive electronic chips is rapidly increasing. The primary growth drivers come from advancements in power management ICs, sensors, and analog ICs, while electric and energy vehicles continue to boost the growth momentum for automotive ICs.

To ensure that automotive electronic chips function properly under various complex conditions while safeguarding the safety of drivers and passengers, iSTART-TEK has developed customized eFlash testing IP and repair IP. These solutions not only shorten the eFlash testing time and fully meet the necessary testing requirements but also help reduce chip testing costs.

iSTART-TEK's customized eFlash testing and repair IP meets the specific testing and repair demands of many well-known semiconductor manufacturers. Users can integrate this customized eFlash testing and repair IP into their SoCs.

Currently, iSTART-TEK's eFlash testing and repair IP has been adopted by chip suppliers for Chinese new energy vehicle manufacturers.

**Advantages of eFlash BIST IP**

- It helps customers reduce development time for implementing eFlash testing and repair circuits.
- It fully meets the complete testing requirements for eFlash.
- It shortens eFlash testing time.

iSTART-TEK's solutions help automotive electronic chip suppliers complete eFlash testing and repair tasks, significantly shortening automotive chip development time, enhancing driving safety, and reducing chip testing costs.

The use of IP has become an indispensable part of SoC design, and iSTART-TEK's customized eFlash testing and repair IP fully meets customers' needs for improving chip quality while reducing costs.

# iSTART-TEK Provides Design Services to EDA tool and IP Licensing Customers

Specializing in EDA tools and IP, iSTART-TEK provides comprehensive design services to EDA tool and IP licensing customers to help them overcome time pressures and burdens in chip development and save time.

## Back-End Service

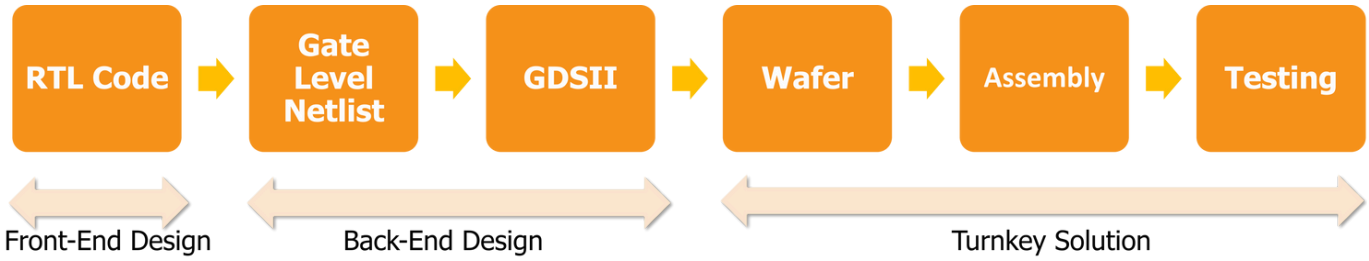
The Back-End Service cover design processes including SRAM BIST/BISR, Scan Chain Insertion, Logic BIST, Automatic Place and Route (APR) and Automatic Test Pattern Generation (ATPG). After the processes mentioned above are completed, iSTART-TEK will provide customers with GDSII document for subsequent manufacturing and testing.

## Spec-in Service

iSTART-TEK provides spec-in service tailored to customer needs, including SoC architecture design, system integration and verification, power and performance evaluation, and system prototyping.

## Fabrication Service

iSTART-TEK's design service also include Multi-Project Wafer (MPW) and Tape-Out services.




## Success Story

iSTART-TEK's design services have successfully realized chip mass production of TSMC's 22 nm, 12 nm and 7 nm technologies. Its customers' end products are used in AI, ADAS, Automotive Blocks, and WiFi.

| Process | Foundry | Key Features |
|---|---|---|
| 7nm | TSMC | Automotive Block |
| 7nm | TSMC | AI |
| 12nm | | |
| 12nm | TSMC | Automotive ADAS |
| 22nm | | |
| 22nm | TSMC | WiFi |

With these success cases, iSTART-TEK's design services have proven to increase customer loyalty and provide higher quality services.

# Ensure Chip Lifecycle with the EZ-Monitor IP

It is crucial to ensure the accuracy of memory operation over long periods as safety specifications continue to evolve.

EZ-Monitor IP is an IP designed for memory testing in the function mode. It supports Soft Repair and can coexist with existing MBIST (Memory Built-in Self-Test) circuits. This Soft Repair technology enhances chip resilience, and the compatibility of EZ-Monitor IP with MBIST circuits brings greater convenience and flexibility to applications.

## EZ-Monitor IP Workflow

EZ-Monitor IP circuits can coexist with existing MBIST circuits, and be inserted beside the critical memory that need to be tested in the function mode, as shown in Figure 1. We can use multiplexers to switch the SRAM control signals, use ezm_MEN as the enable signal, and connect to the top through the Basic I/O interface. Note that the circuit insertion rule follows the clock domain.

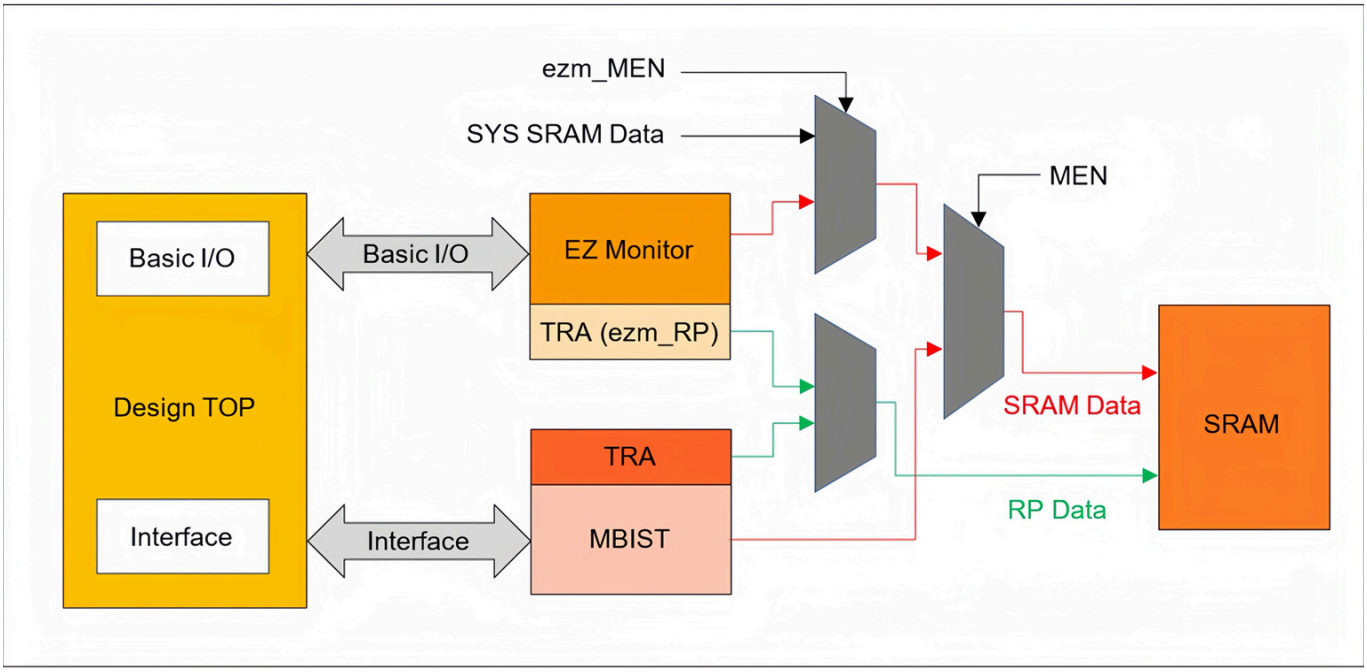


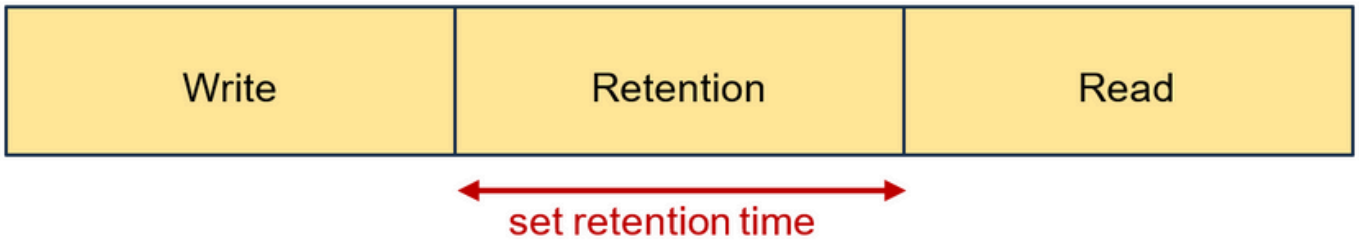

Figure 1 EZ-Monitor IP Workflow

## EZ-Monitor IP Algorithms

EZ-Monitor IP adopts the retention test algorithm, which inserts a retention state between the read and write operations. EZ-Monitor IP supports two methods. The first one involves a fixed retention time. The retention time is pre-programmed into the circuit, resulting in a constant retention time for all tests. The second method uses a handshake mechanism.

Through an interface, EZ-Monitor IP sends out RET state signals and enter the retention period after finishing the write operation of the memory testing data. When users are ready to end the retention period, the interface sends out an RET done signal and initiates the read operation, as shown in Figure 2.

Fixing retention time:




Handshake:

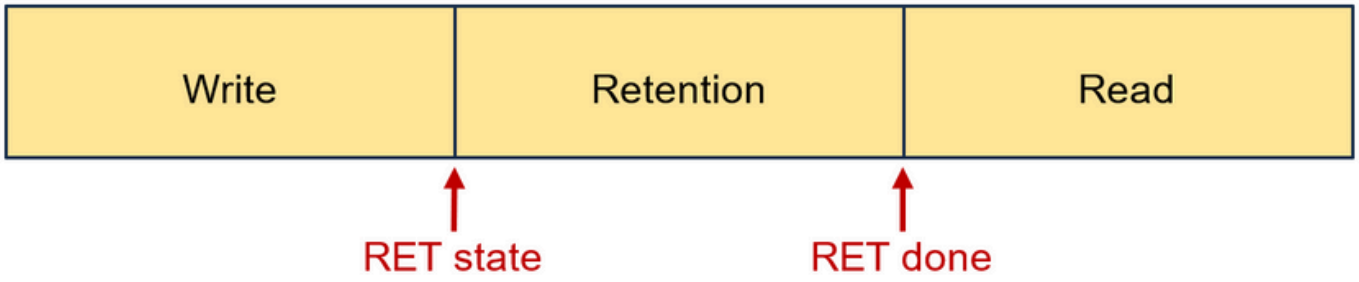



Figure 2 EZ-Monitor IP Algorithms

## EZ-Monitor IP Waveforms

The fixed retention time waveform is shown in Figure 3.

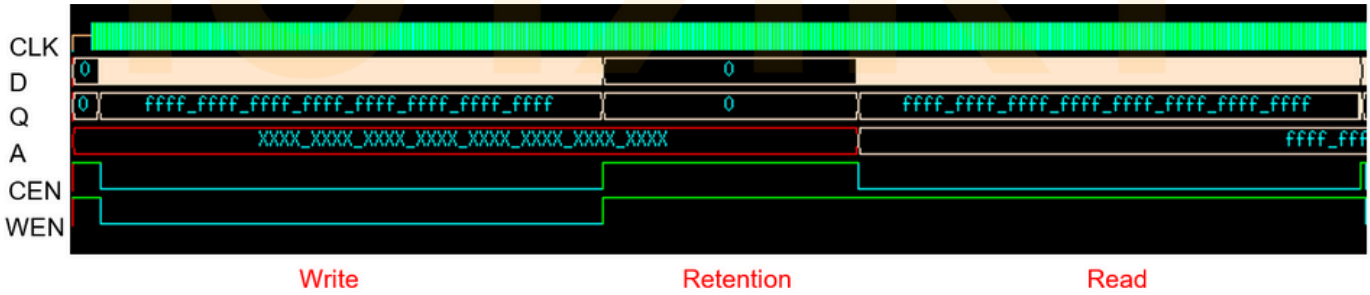



Figure 3 The Fixed Retention Time Waveform

The handshake waveform is shown in Figure 4.

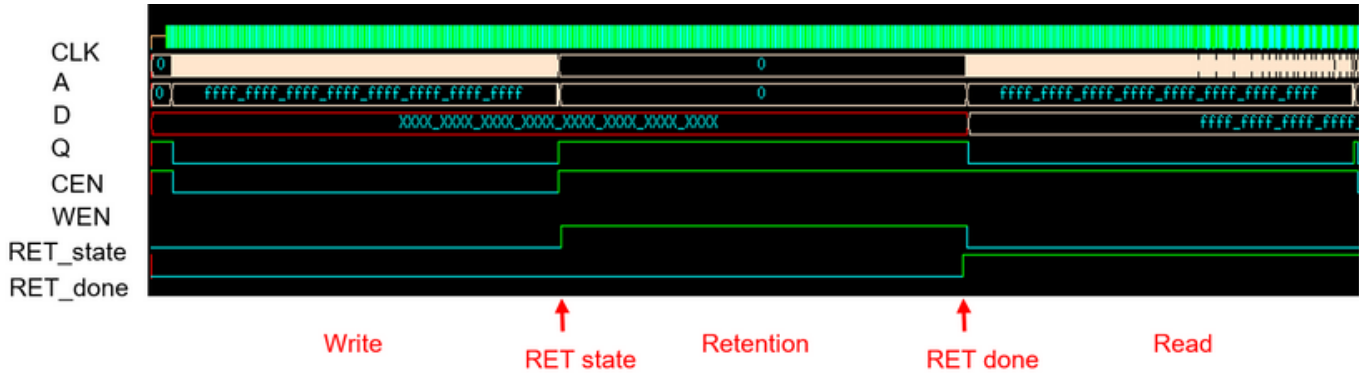



Figure 4 The Handshake Waveform

Firstly, execute the normal test driven by the input signal, ezm_RP_default_MEN_D, including two background data (0F/5A). After memory faults are detected and the repair data is provided, the repair and re-test actions are performed.Figure 4 & 5 shows the retention handshake waveforms with Soft Repair.

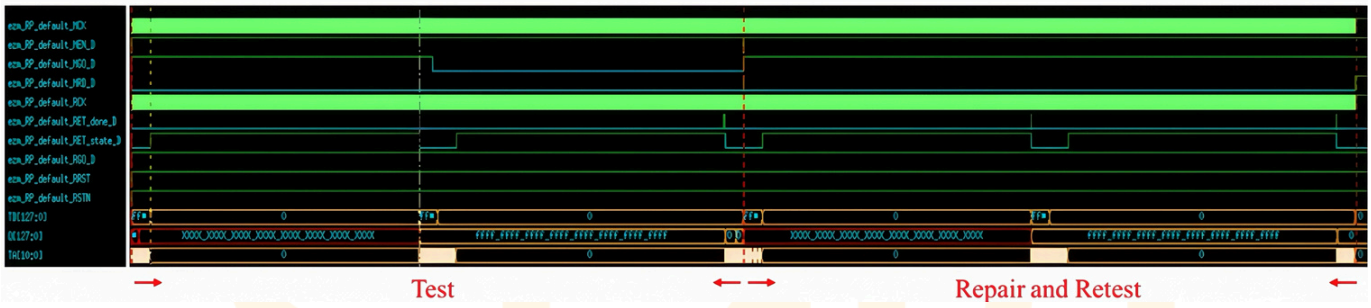



Figure 5 The Waveform of EZ-Monitor IP Interface (1)

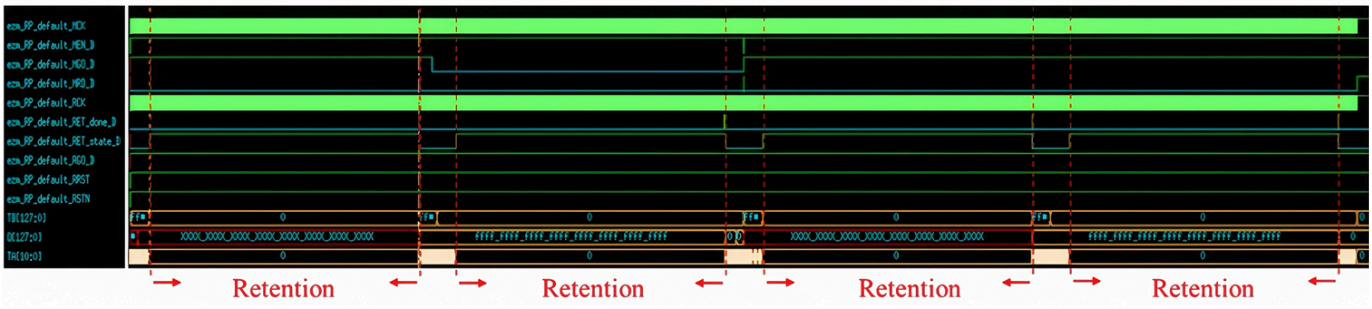



Figure 6 The Waveform of EZ-Monitor IP Interface (2)

## EZ-Monitor IP Interface

EZ-Monitor IP supports the Basic I/O interface. The ezm_MEN signal serves as the enable signal for the circuit, while ezm_RET_done functions as the control signal for the handshake mechanism. The ezm_MGO signal provides the result of the memory test, and finally, ezm_RGO determines whether memory repair can be performed, as shown in Figure 7.

| Signal | Descriptions |
|---|---|
| ezm_MCK | ez Monitor controller Clock |
| ezm_MEN | ez Monitor controller Enable |
| ezm_MGO | ez Monitor test pass/ fail |
| ezm_MRD | ez Monitor finish test |
| ezm_RSTN | ez Monitor reset (active low) |
| ezm_RET_state | Retention start |
| ezm_RET_done | Retention finish |
| ezm_RGO | Repair available (Repair) |
| ezm_RRST | Repair reset (Repair) |
| ezm_RCK | Repair controller clock (Repair) |

Figure 7 EZ-Monitor IP Interface