iSTART iReport

iSTART TEK INC.

Patent

News

White Paper

iSTART Class

iSTART-TEK Obtains U.S. Patent "METHOD FOR GENERATINGAN MEMORY BUILT-IN SELF-TEST ALGORITHM CIRCUIT"

iSTART-TEK has successfully obtained the U.S. patent for "METHOD FOR GENERATING A MEMORY BUILT-IN SELF-TEST ALGORITHM CIRCUIT"! iSTART-TEK's self-developed User-Defined Algorithm (UDA) adopts the architecture outlined in this patent.

Commonly used memory testing algorithms on the market currently exhibit behaviors of repetitive testing, requiring additional testing time and costs. Simultaneously, with the continuous evolution of technology, advanced manufacturing processes are consistently emerging. Existing algorithms may not be capable of detecting memory defects in these advanced processes, failing to meet the demands of staying up-to-date.

iSTART-TEK's new patent can effectively addresses this situation. By utilizing UDA, redundant elements can be eliminated. Users can edit algorithm files, define memory locations, significantly reducing memory testing time. Additionally, UDA allows the design of more complex and area-efficient memory testing algorithms, offering greater flexibility and diversity.

After obtaining a Taiwanese patent in 2022, this technology successfully secured a U.S. patent in October 2023. This not only acknowledges iSTART-TEK's research and development capabilities but also instills confidence in its ability to assist customers in resolving memory testing challenges and improving design and production efficiency.

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iSTART-TEK Targets Automotive Electronics with Customized EDA Tools

In recent years, the semiconductor industry has gained global attention, driven by international affairs, geopolitics, and economic development. The semiconductor supply chain is working to overcome challenges and explore new business opportunities. EDA, as a crucial tool for chip design, has emerged as a top priority within the semiconductor sector. iSTART-TEK focuses on memory testing and repair technology within the EDA industry. With the growing trends in AI, automotive electronics, IoT, and industrial applications, the complexity of IC design has substantially increased, providing ample opportunities for development in the EDA industry.

"iSTART-TEK specializes in developing advanced automated EDA tools," said Nico Wang, Vice President of iSTART-TEK. "We are actively integrating cloud services and AI into our EDA tools. This flexible cloud solution is designed to significantly enhance work efficiency and reduce project completion time. The highly automated GUI interface ensures user-friendly operations. Through a commitment to high automation, innovative cloud technology, and real-time services, iSTART-TEK has secured a leading position in the global industry."

Nico Wang mentioned that iSTART-TEK is strategically expanding its market and adopting a comprehensive approach to enhance their competitiveness. For instance, recognizing the potential of China's growing semiconductor market, iSTART-TEK established a subsidiary in Shanghai in 2022 to bolster their technical services. This move aims to seize the EDA market in China, establishing a robust and diversified foundation for iSTART-TEK's development. Moreover, they are strategically broadening their global presence, conveying iSTART-TEK's expertise and core values worldwide.

Hermes Chang, Senior Director of iSTART-TEK Finance & Accounting Division, shared that iSTART-TEK achieved an outstanding year-over-year growth of 146% in 2022. Despite a global economic downturn in 2023, its revenue from January to October of the same year increased by 76.6% compared to the previous year. This remarkable performance highlights the sustained demand for EDA tools even in challenging market conditions, affirming customer confidence in iSTART-TEK's offerings. Currently, all members of the iSTART-TEK team are diligently working towards going public. Their goals are not only to attract top talents but also to expand the reach of their EDA tools, diversify our product line, explore new market opportunities, and generate greater profits to reward their shareholders.

During the COVID-19 pandemic, iSTART-TEK faced a downturn in revenue. TP Hsieh, Senior Director of iSTART-TEK Technical Support Division, mentioned that despite stringent isolation

policies at the time, the company remained proactive in visiting clients. The reason is automotive electronics and High-Performance Computing (HPC) have significant growth potential in the future. That is why iSTART-TEK is focusing on the development of memory self-test circuits for automotive electronics and HPC. Its well-developed functions including POT (Power_On Test), MSW (Memory Status Watch-Dog), Circuit Self-Verification (CSV), Automatic Repairing Flow (ARF) and Testing Element Configuration (TEC) enable customers to enhance their product competitiveness.

Dedicated to technological advancements and providing attentive technical support, iSTART-TEK has seized opportunities for business growth under the challenges of the industry trend.

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Highly Configurable RRAM IP Testing and Repairing Circuits Development Environment: EZ-NBIST

1. **Testing methodologies of RRAM IP**

The testing methodologies of RRAM IP cover full wafer sorts, and the final test for UMC's 22nm process and customized embedded RRAM IPs. Thus, iSTART-TEK develops the EZ-NBIST GUI tool to help users reduce BIST coding time of RRAM IPs. EZ-NBIST follows RRAM vendors' testing methodologies to implement all test items' timing diagrams and reduce parallel long testing time in ATE.

2. **Why RRAM IP needs to use BIST and BISR**

RRAM IP has complicated testing functions to cover each disturbing condition in the 22nm process. The memory BIST adds logic to an IC, enabling the SoC to autonomously test its own memory operation.

MBIST tests the RRAM macro through an effective test algorithm to detect possibly all the faults. MBIST generates test patterns from RRAM vendors' requirements to the RRAM macro and reads them to find RRAM defects. BISR adds repair circuits to the backup memory to increase the RRAM IC yield.

3. **How iSTART-TEK accomplish BIST and BISR of RRAM IPs**

iSTART-TEK develops the EZ-NBIST GUI tool to generate BIST and BISR of RRAM IPs. iSTART-TEK BIST implements all RRAM test items to cover wafer soft and final tests. The BIST interface is a flexible serial interface to reduce IC test pins. It enhances BIST test flexibility by allowing individual enabling and disabling of all test items. Additionally, it offers a diagnosis mode to debug the defect address.

iSTART-TEK's BISR records faulty RRAM memory addresses and utilizes redundancy to enhance the yield of RRAM ICs. It also offers an auto-repair function.

Figure 1 illustrates the RRAM test and repair solutions.

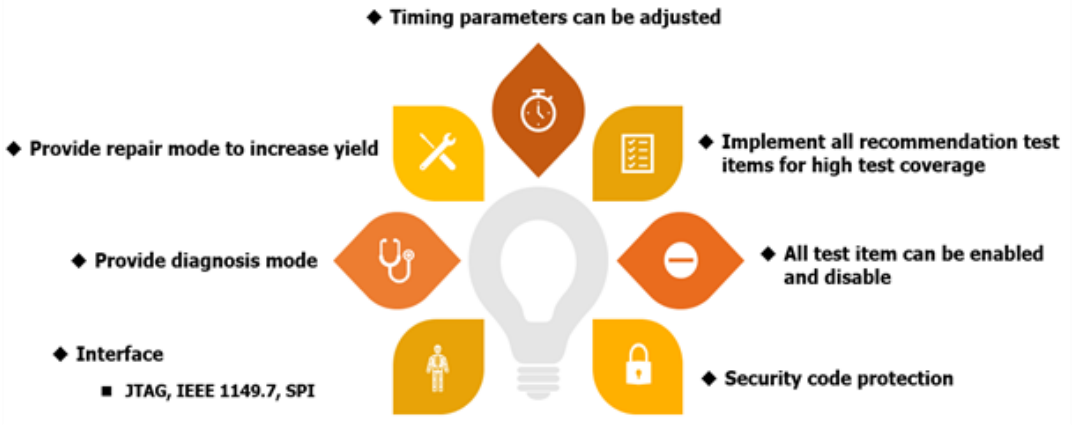

Figure 1

Figure 2 shows RRAM tests and repair features.

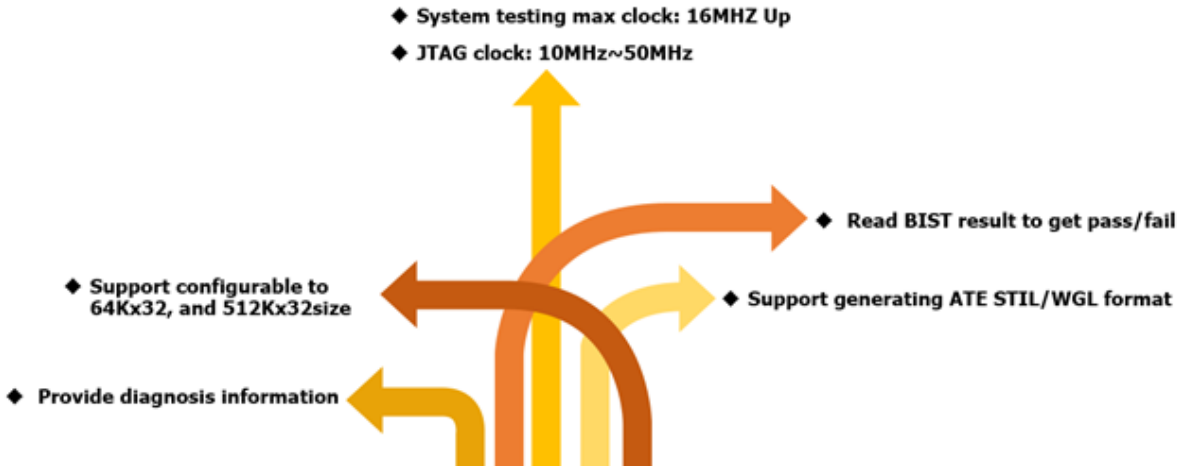

Figure 2

Figure 3 shows the RRAM diagnosis simulation output.

```
tem cnt: 374
ddr:     1
ault_bit:00000000000000000000010000000000

tem cnt: 374
ddr:   255
ault_bit:00000000000000000000010000000000

tem cnt: 374
ddr:   511
ault_bit:00000000000000000000010000000000

tem cnt: 374
ddr:   521
ault_bit:00000000000000000000010000000000

tem cnt: 374
ddr:   541
ault_bit:00000000000000000000010000000000
```

Figure 3

Figure 4 shows the BISR circuit block.

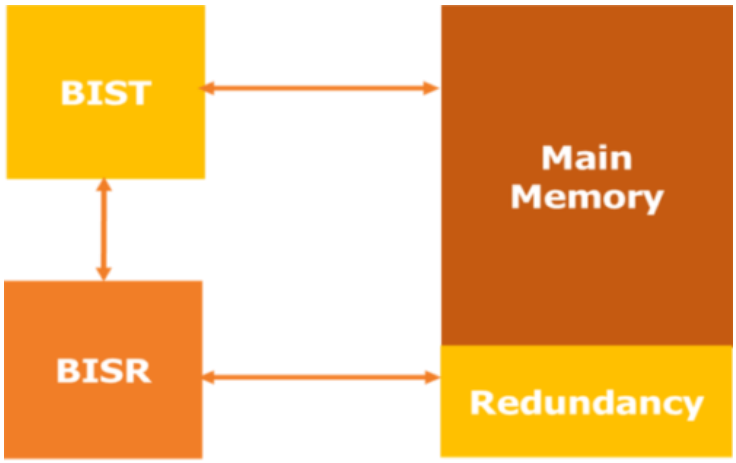

Figure 4

4. **Introduction of EZ-NBIST**

EZ-NBIST is an RRAM GUI tool that can generate BIST and BISR of RRAM IPs. Figure 5 shows the perspective of EZ-NBIST GUI. To access the "EZ-NBIST Config," click on "EZ-NBIST Config" from the "Config" drop-down menu.

Figure 5

Users can click “Run...” from “Run” drop-down menu to execute EZ-NBIST as shown in Figure 6.

Figure 6

5. **How many RRAM IP are included in EZ-NBIST?**

The EZ-NBIST GUI supports various RRAM IPs, including UMC 512Kx32, 64Kx32 IP sizes, and customizable IP sizes. Users have the flexibility to select customized RRAM macro types, vendor types, and specific RRAM macro sizes, as illustrated in Figure 7 and Figure 8.

Figure 7

Figure 8

6. The interfaces included in EZ-NBIST

EZ-NBIST GUI supports 3 flexible serial interfaces JTAG, IEEE1149.7, and SPI as shown in Figure 9.

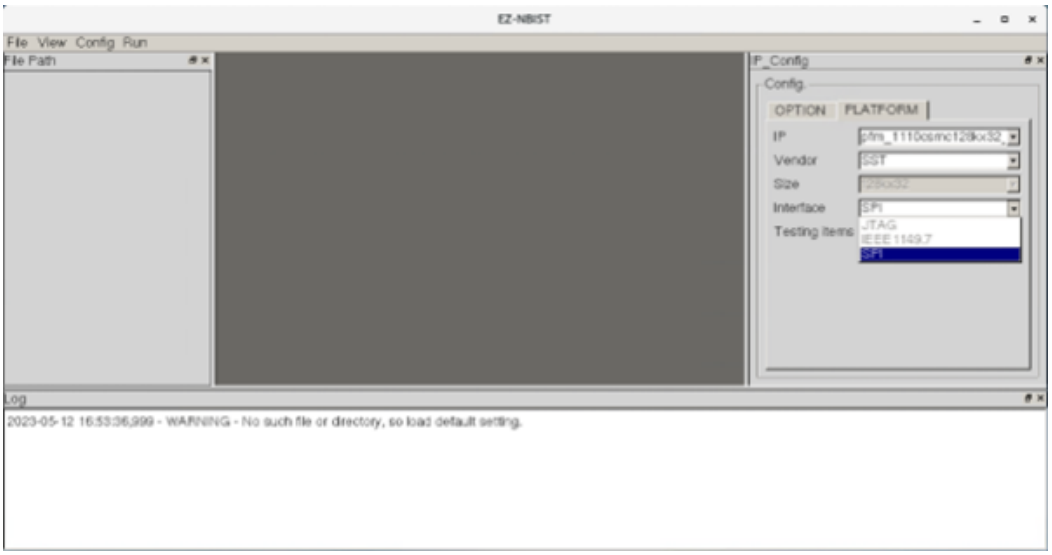

Figure 9

Figure 10 shows the RRAM test and repair block with the IEEE1149.7 interface.

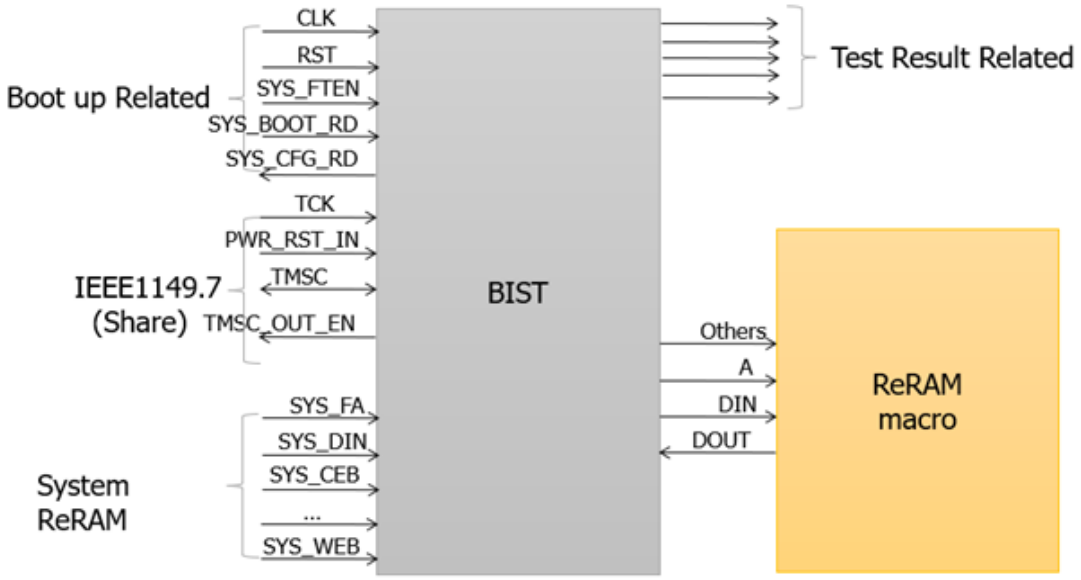

Figure 10

7. The flexibility of EZ-NBIST

EZ-NBIST supports configurable BIST and BISR IP for different RRAM macro sizes. With this feature, all RRAM timing parameters can be adjusted. Figure 11 shows that all test items can be enabled and disabled individually.

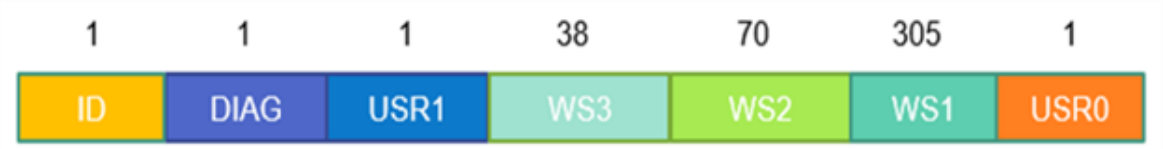

Figure 11

EZ-NBIST can help users generate the complete synthesis RTL, the verification environment, the testing patterns, the behavior model, and the customized RRAM database as shown in Figure 12.

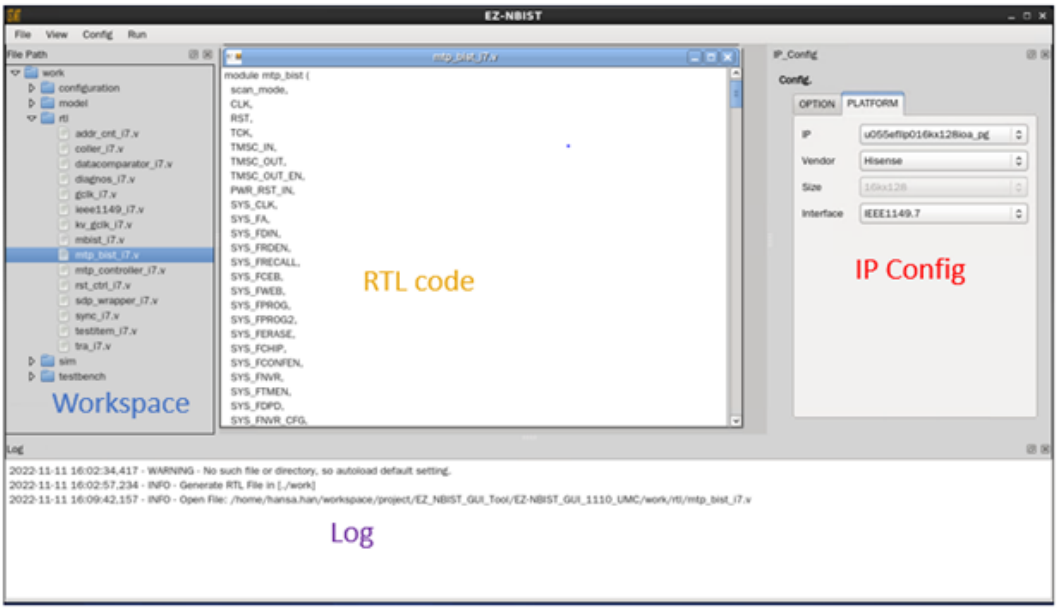

Figure 12

To execute simulation with RRAM model, users can select a test pattern to generate simulation dump files. For example, as Figure 1 shows, execute “2” into start “ws1” testing item’s simulation flow.

8.Conclusion

EZ-NBIST offers professional testing items for RRAM BIST/BISR. It efficiently saves RRAM tuning parameter timing time in ATE. The area overhead of RRAM BIST and BISR on the SoC is deemed acceptable. Additionally, EZ-NBIST is user-friendly and easy to set up, facilitating the testing circuit for RRAM IPs.

iSTART Class Episode 1: BIST & BISR

The impact of BIST & BISR on SoCs?

Let's start with the recent trending topic, ChatGPT. ChatGPT belongs to AI applications, requiring high-end CPUs or GPUs for processing. These complex AI operations demand substantial memory usage. To ensure memory operates correctly, once SoCs are produced in the wafer factory, BIST is utilized for testing. If any memory issues arise, BISR is employed for repair.

Presently, AI wafer production involves advanced processes. Apart from potential static defects, advanced process SoCs might also encounter dynamic defects. Therefore, effective BIST self-testing circuit designs should precisely detect both static and dynamic defects. However, BIST only identifies defects. To transform flawed wafers into usable chips, a repair solution is essential. Through BISR circuits, faulty memory is replaced with reliable redundant memory, allowing the wafer to resume normal operations.

iSTART-TEK is a professional memory BIST & BISR EDA tools provider with nearly 40 patents. Through our EDA tools, we achieve “APA”, which stand for Algorithm, Performance & Area. This means that iSTART’s tools can offer many kinds of memory testing algorithms with excellent execution efficiency, resulting in the smallest BIST & BISR circuit area.

iSTART-TEK is currently the only memory BIST & BISR EDA tools vendor in Asia, providing tools suitable for all kinds of application of IC designs. Our customer base includes applications in AI, automotive, mobile phones, networks, displays, and more.

Based on customer feedback, iSTART-TEK’s tools have demonstrated fast and accurate generation of memory BIST & BISR circuits in many types of SoC chips.

This enables the detection of memory defects, effectively improving the quality and yield of customers’ SoC chips.

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iSTART Class Episode 2: Testing Algorithms

What is the difference between “static faults” and “dynamic faults”?

"Static failure" and "dynamic failure" are two types of errors in memory. To put it simply, the distinction between them lies in how and when the faults occur. Static failure is a fault that can be detected in a single operation, like an obvious error that occurs when manipulating the memory, such as pressing a button with no response. For instance, if a memory unit can only output "0" permanently without any changes, this is a form of static failure.

On the other hand, dynamic failure requires multiple operations to be triggered, similar to a more complex issue that needs specific conditions or operations to manifest. For example, a memory unit may only exhibit an error after multiple read and write operations under certain conditions.

In summary, the main difference between static and dynamic failure lies in how the errors manifest. Static failure is evident and can be discovered with a single operation, while dynamic failure requires multiple operations under specific conditions. However, it's worth noting that static failure may occur in various processes, while dynamic failure typically arises in higher-level processes. With many applications gradually moving towards advanced processes, this is also a trend worth monitoring.

For example, there is an algorithm called "March C" used to detect static failures in memory. March C induces different states in memory units through a series of read and write operations, verifying whether the previous states are correct after each operation. If an error occurs at a specific step, it indicates the presence of static failure. In short, March C helps identify memory issues that can be discovered with single operations through a specific sequence of actions.

There is another algorithm called "March 33N," which is used to identify dynamic failures. March 33N has a relatively high complexity and induces changes in memory cells through a series of read and write operations along with specific steps over multiple cycles. After each operation, the algorithm performs a read operation to check for any unexpected faults. If errors occur in the memory after specific operations, it indicates the presence of dynamic failures.

In addition to various algorithms, there are different testing methods. For example, the "Checkerboard" testing method involves alternating writes of "0" and "1" between memory cells, followed by read operations to check for errors. This method helps identify dynamic failures that require multiple operations to be triggered.

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iSTART Class Episode 3: EZ-Debug

The function and efficiency of EZ-Debug

EZ-Debug is a board directly connect with the PC and FPGA, and on the PC we can easily use a few clicks to control the FPGA/IC to do the test. What we do is to check if any failure exists in the circuits, it can directly show the location of the failure. This is called “architecture”.

Usually, companies purchase ATE (Automatic Test Equipment) to do the auto test for IC. However, using iSTART-TEK’s memory diagnosis tool, EZ-Debug, is more cost-effective cand can bring higher efficiency. If your interface is IEEE1500, the upper limit of speed is 30MHzm, meaning it sends 30 million signals into the EVB board in one second.

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iSTART Class Episode 4: iSTART-TEK Technical Service

Customer service offerings provided by iSTART-TEK

Our customer service offerings are divided into online and offline categories. Online services include information available on our official website. By clicking on the "Technical Support" section on iSTART-TEK's official website, users can access technical articles, document downloads, and technical forums as well as the workshops. Technical articles cover the usage and functionalities of various product tools, along with their applications. The primary focus is on the transfer and promotion of technical knowledge. Document downloads provide user manuals and related documents for our tools, while the technical forum on the workshop platform not only allows customers to download tools but also provides detailed explanations of each tool's functions and answers to frequently asked questions.

Additionally, we regularly conduct webinars and produce videos for the iSTART Class. Each webinar introduces different topics, catering to specific interests, while iSTART Class videos offer a concise overview of MBIST principles suitable for a general audience.

Offline support involves direct technical assistance, including phone calls, emails, and direct communication with our Research and Development (RD) team. RD may also provide on-site support to clients, covering practical implementation of real cases or offering educational training on tool usage. Furthermore, we organize physical iSTART-TEK Design Workshops, inviting clients to learn about our solutions, including tool operations and in-depth technical discussions. Our RD team is present to answer questions and provide support during these workshops.

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iSTART Class Episode 5: START & EZ-BIST

iSTART-TEK's automated memory test and repair EDA tools

iSTART-TEK provides a range of automated memory testing and repair EDA tools. Among its main product lines, iSTART-TEK offers EDA tools like START, capable of rapidly generating memory test and repair circuits. START stands for SoC's Memory Test and Repair Technology. "Test" refers to memory testing functionality, while 'Repair' encompasses efficient memory repair technologies, including Hard-Repair and Soft-Repair. Both repair methods significantly enhance chip yield.

iSTART-TEK's products apart from START

Let's talk about another EDA tool commonly associated with START – EZ-BIST. Other products will be introduced in the upcoming episodes, so stay tuned! The major difference between EZ-BIST and START is that EZ-BIST specifically focuses on the development of memory testing circuits. The main reason behind this is the diverse needs of different applications, and iSTART-TEK aims to provide users with tools that best meet their requirements. Notably, to ensure the ease of use implied by its name, EZ-BIST also supports a GUI mode. This allows users less familiar with commands to operate more intuitively and efficiently through a graphical interface. Additionally, for those unfamiliar with algorithms or uncertain about which algorithm to choose, EZ-BIST can provide algorithm recommendations based on the user's selected application – truly making it "EZ"!

What other advantages do START and EZ-BIST offer?

Apart from holding nearly 40 patents in memory testing and repair technology, both START and EZ-BIST provide various automation features. These include Memory Auto-Identify, Clock Tracing, and Memory Auto-Grouping. Auto-Grouping can be performed using default settings or customized according to user needs under different conditions. These advantages significantly reduce the time spent on manual configuration and modifications, allowing users to significantly shorten the chip development timeline. Furthermore, we offer diagnostic features, EZ-Debug, and a data analysis platform for ATE machines, enabling chip developers to conveniently and rapidly obtain diagnostic analyses and results post-memory testing. iSTART-TEK's EDA tools also offer advanced features tailored for applications such as automotive electronics and high-performance computing chips. We will delve into these features in more detail in upcoming episodes.

iSTART-TEK's automated EDA tools, START and EZ-BIST, not only assist IC design companies in effectively improving chip yield but also expedite the development timeline for memory testing and repair circuits through a range of functionalities. In the next episode, we will explore the features provided by iSTART-TEK's products in applications related to automotive electronics and HPC chips.

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iSTART Class Episode 6: Customer Testimonial - iTE

iTE has been a longstanding partner of iSTART-TEK. How have iSTART-TEK's products benefited in enhancing the performance of iTE's chips?

Using iSTART-TEK products has significantly boosted ITE's chip performance. Their choice of ISTART-TEK as a partner was driven by competitive pricing and flexible support, especially in customization. For instance, the initial implementation of memory repair in 8-inch mature processes increased overall yield from 90% to 94.3%, with a mere 0.3% area increase.

ISTART-TEK's diverse testing interfaces, supporting JTAG or Basic I/O based on product needs, have been a game-changer. Their user-friendly tools seamlessly integrate into ITE Design Flow, reducing DPPM and increasing yield.

The applications of iTE’s chips

ITE's chips are mainly used for PC/NB products. Additionally, their products like Video Bridge and SoCs, heavily reliant on SRAM, benefit from ISTART-TEK's technology.

ISTART-TEK, committed to technical excellence, aims to assist more IC design companies in elevating chip yield, shortening development cycles, and reducing costs. If you’re interested in memory testing and repair, connect with us for the most professional automated solutions and product services. Check out our website for more product information, and feel free to reach out with any inquiries!

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iSTART Class Episode 7: Customer Testimonial - Rafael Micro

How iSTART-TEK’s products benefit Rafael Micro’s chips

We have interviewed with Rafael Micro, iSTART-TEK's valuable customer, for the experience of using iSTART-TEK's EDA tools. In the intricate world of wafer manufacturing, navigating through various memory defects is inevitable. For mid-sized IC design houses like Rafael Micro, developing in-house memory test processes can be a challenging task but a necessary one. Using iSTART-TEK's products makes Rafael Micro 's IC design development more flexible and focused, especially in the field of wireless communications. iSTART-TEK's Memory BIST automatically identifies IC memory defects during mass production testing, while Memory BISR successfully repairs defective memory, reducing 30% of product defects caused by memory issues. This enhances Rafael Micro 's yield and testing process control for advanced SoCs in the future.

The applications of Rafael Micro’s chips

Specializing in wireless communication, Rafael Micro's products includes TV Tuners and IoT devices. TV Tuners, crucial for video transmission, heavily rely on SRAM for storage. As IoT SoCs thrive in the era of IoT and AI, the demand for SRAM for networking information and computation storage increases. Hence, the collaboration between iSTART-TEK's products and Rafael Micro 's offerings is set to become even more integral in the future.

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iSTART Class Episode 8: Specific functions for Automotive and HPC

What features do iSTART-TEK's EDA tools provide for automotive electronics and HPC chips?

For automotive electronics chips, we offer features such as Power-On Test, Error-Correcting Code, and Testing Elements Change. POT can be implemented in different ways, including recording the test process in ROM to control the test commands, using RTL or a signal to control, and implementing it through the CPU. If using the CPU, it enables "Memory Status Watch-Dog," allowing immediate memory testing and repair after powering on the chip. It ensures repaired memory operates correctly by testing it immediately. Additionally, POT includes "BIST Circuit Self-Verification," which involves self-checking the accuracy of the memory test circuit through the Error Injection mechanism. ECC is used to ensure data correctness during the runtime of the system, and TEC optimizes memory test algorithms by flexibly adjusting memory test units. These features focus on enhancing and ensuring security, meeting safety requirements for automotive electronics application.

What customized solutions for HPC chips are provided?

In addition to providing POT, we offer Multi-Chain, Power Consumption Analysis Mechanism, and Memory Group Based on Layout Definition File for HPC application. Multi-Chain allows users to plan any number of chains based on SoC design requirements, controlling power consumption and transmission speed through multiple repair chain functions for diverse SoC designs. PCA manages the power consumption of memory groups based on memory power consumption information. When the total power consumption of grouped memory exceeds the SoC's power limit, it automatically reorganizes memory groups. MGD allows users to create a memory grouping mechanism based on existing layouts. These features, along with previously introduced POT and TEC, are solutions customized for HPC chips.

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iSTART Class Episode 9: EZ-Safety & EZ-TEC

What IP products are ISTART-TEK going to launch?

The first one is EZ-Safety. As mentioned in the last episode, iSTART-TEK's EDA tools offer various features to enhance safety for automotive-related chips. Safety is crucial in the field of automotive electronics. Therefore, in addition to the EDA tool product line, iSTART-TEK continues to develop IP products like EZ-Safety. EZ-Safety adjusts the traditional MBIST architecture, allowing it to operate independently within the existing MBIST framework. It extracts several important signals needed for memory testing, making memory detection more efficient. It automatically backs up specified memory information, and testing is not limited to the test mode only, contributing to overall safety improvement. Moreover, EZ-Safety highlights easy and intuitive insertion and integration. It not only enhances real-time and flexible memory testing but also specifically supports testing algorithms suitable for automotive applications.

What is the other new product?

The other upcoming IP product is EZ-TEC. Similar to EZ-Safety, it can independently operate within the existing MBIST framework and is easy to insert and integrate into designs. The implemented MBIST architecture of EZ-TEC has the capability to dynamically adjust memory test algorithms. We previously covered algorithms and memory failures in an episode. With EZ-TEC, designers can go beyond well-known common algorithms and customize testing algorithms down to the element level based on individual requirements. This customization aims to improve chip yield.

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