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iSTART-TEK's "Configurable ATE Tool Flow" Granted a Utility Model Patent

This innovative tool flow is specifically designed to analyze memory testing results and reduce memory testing file transfer time. With this technology, all memory testing results within the SoC can be efficiently analyzed. Complemented by iSTART-TEK's suite of EDA tools, including STIL patterns, meminfo (for recording memory testing data and algorithms), testbench (which facilitates circuit simulation and testing export data), and the testing results generated by an ATE, the "Configurable ATE Tool Flow" enables comprehensive testing of all memories within an SoC and analysis of memory error information. This delivers enhanced convenience and efficiency in memory testing services for customers.

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中華民國專利證書

新型第 M652657 號

新型名稱：測試結果分析裝置

專利權人：芯測科技股份有限公司

新型創作人：洪期煌、陳政旭

專利權期間：自2024年3月11日至2033年10月17日止

經濟部智慧財產局局長 廖承威

中華民國 113 年 3 月 11 日

iSTART-TEK Introduced Two Specialized IP Products for Memory Testing

As Asia's only developer for memory testing and repair technologies, iSTART-TEK exclusively provides the solutions and customized design services. Its main products include EDA tools and IP (Intellectual Property). As the semiconductor industry gradually recovers, chip design companies are shifting towards a diversified business model, focusing on the development of various chips. Fields such as automotive electronics chips, artificial intelligence chips, ChatGPT-related chips, IoT chips, and consumer product chips have become battlegrounds for chip design companies. Therefore, standing out among numerous chip design companies and ensuring both the design quality and pricing of chips have become crucial factors.

In the first quarter of 2024, iSTART-TEK launched two IP products specializing in on-chip memory testing, namely EZ-Safety and EZ-TEC.

EZ-Safety is a dedicated IP designed for automotive electronic chips. It can meet the ISO 26262 specifications and assist automotive chip design companies in developing chips that comply with ISO 26262 standards more efficiently.

EZ-Safety can coexist with the existing memory testing circuits of automotive chip design companies, and conduct memory testing for the critical memories within automotive electronic chips. Prior to performing the critical memory tests within automotive electronic chips, EZ-Safety automatically backs up the data within those memories. Once EZ-Safety completes the testing process for the memory, it automatically restores the backed-up data to the memory if the read and write operations are error-free. However, if errors occur during the read and write operations of the memory, EZ-Safety will notify the chip's control system, such as the CPU.

EZ-Safety is easy-to-use. Simply by linking EZ-Safety with the critical memories within automotive electronic chips, EZ-Safety will automatically complete data backup, memory testing, and data restoration.

The other IP product is EZ-TEC (Testing Element Change), which is a dedicated IP for memory testing designed based on iSTART-TEK's U. S. patent "METHOD FOR GENERATING AN MEMORY BUILT-IN SELF-TEST ALGORITHM CIRCUIT".

EZ-TEC can coexist with the existing memory testing circuits of chip design companies. This U. S. patent breaks down memory testing algorithms into elements, allowing users to reconstruct the architecture of any memory testing algorithm through element reorganization. With EZ-TEC, users can select the elements of the memory testing algorithm for the critical memories within the chip. After completing the CP (Chip Probe) test, if memory defects persist in the critical memories of the chip, chip design companies can use the JTAG (Joint Test Action Group) interface to rearrange the selected elements through permutations and combinations. This process forms a new memory testing algorithm. Subsequently, the chip can undergo testing for the critical memories using the new memory testing algorithm, effectively reducing the DPPM (Defective Parts Per Million).

The usage of EZ-TEC is straightforward. By simply connecting EZ-TEC to the critical memories within the chip and selecting the elements of the memory testing algorithm to be used, users can redesign the memory testing algorithm through JTAG. This allows for the post-production adoption of a new memory testing algorithm for the critical memories within the chip, along with a retesting of these critical memories to enhance chip quality.

EZ-Safety is an IP designed for automotive electronic chips, enabling automotive chip design companies to easily comply with ISO 26262 specifications for automotive electronic chips. It assists chip development companies in changing the memory testing algorithm even after production. This is particularly valuable for addressing situations where critical memory defects were not detected during the CP stage. By conducting a retesting of these critical memories with a new memory testing algorithm, EZ-TEC effectively reduces DPPM and improves chip quality.

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START™ v3's Crucial Role in AI, HPC and Automotive Electronics

The flourishing fields of AI, HPC and automotive electronics is driving the resurgence of the semiconductor industry and development of future technologies. Both AI and HPC demand the use of CPUs to execute computing tasks for processing operating systems and applications, relying heavily on a large amount of SRAM. iSTART-TEK's EDA tool, START™ v3, designed for memory testing and repair, excels in SRAM repair with OTP, meeting the industry's requirements amid this prevailing trend. Based on an innovative patented architecture, START™ v3 features high-efficiency memory repair technology and sophisticated memory testing algorithms. It accurately identifies the memory defect locations and fix them in a short time. The Hard-Repair feature enables efficient memory repair with OTP, enhancing yields, reducing costs for HPC, AI, and automotive electronics chips, thereby boosting product competitiveness. iSTART-TEK will continuously be dedicated in technology development and innovations, providing AI, HPC and automotive electronics chips with high-performance memory testing and repair solutions.

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iSTART-TEK Certified with DEKRA's ISO 26262 Professional Functional Safety Engineer Automotive

As technology advances, intelligent electric vehicles not only provide driving convenience but also drive continuous innovation in automotive electronics and related software. To ensure the safe implementation of these innovative technologies and gain consumer trust, ISO 26262 becomes even more critical. Recently, some of iSTART-TEK' s staff obtained certification as Professional Functional Safety Engineers in Automotive from DEKRA, further elevating the company' s outstanding performance in automotive electronics.

ISO 26262 Road Vehicles — Functional Safety is a standard designed for the functional safety analysis of automotive electronics. It covers the whole product lifecycle, including the safety concepts at the initial stage, the system development stage and other crucial stages. iSTART-TEK actively participates in the ISO 26262 Professional Functional Safety Engineer Automotive professional training, contributing to the enhancement of expertise in functional safety for relevant global companies in the automotive industry.
Functional safety engineers of automotive play core roles while a company imports the ISO 26262 standard. They oversee the implementation of routine functional safety measures, ensuring compliance with ISO 26262 specifications to guarantee product reliability and automotive safety. Their active involvement in product development and quality control has contributed to iSTART-TEK' s strengthened position in automotive electronics. iSTART-TEK can now offer more robust technical support in automotive electronics safety.

Learn More

iSTART-TEK Showcased Advanced Memory Testing and Repair Solutions at in the Spring Technical Exchange Conference in Wuxi

iSTART-TEK is honored to be invited to participate in the Spring Technical Exchange Conference held by CR Micro on March 11, 2024. During the conference, we will introduce iSTART-TEK's comprehensive memory testing and repair solutions, along with our latest technological innovations.

Episode 10: Solutions to Complex IC

What is the usage and purchasing method for EZ-Debug?

In traditional IC testing, especially MBIST testing, ATE machines are usually required, which brings additional costs and time. However, by using EZ-Debug, we can quickly and effectively perform MBIST testing, especially during IC trial production or small amount production. It's very convenient to operate, as users can use MBIST tests directly through a PC with simple operations, eliminating the need for complicated ATE machine steps. This not only simplifies the testing process but also significantly reduces related costs. To purchase EZ-Debug, please contact the sales team at iSTART-TEK.

What about the usage timing and advantages of Diagnosis?

Diagnosis is mainly used to analyze memory failures. Through this diagnostic feature, we can obtain information related to failures, including under which algorithm it was detected, like which operation or element, error address, and data, etc. Developers can analyze the Diagnosis information and provide feedback to the chip manufacturers to improve yield rates.

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Episode 11: iSTART Cloud

What is the subscription-based cloud EDA tool service platform?

The subscription-based cloud EDA tool service platform is a new platform that allows users to run EDA tools in a cloud environment. Users only need to complete the corresponding VPN connection settings and then can easily use iSTART-TEK's developed EDA tool – EZ-BIST through a browser connected to the cloud desktop environment. Additionally, the platform offers convenient file upload and download methods, allowing users to upload files to the cloud and also easily download them to their local machine after completing the MBIST circuit.

How does the subscription-based cloud EDA tool service platform ensure security?

The EDA tool service platform with chip Testing Technology's subscription-based cloud has stringent requirements for data security. For the security of the member website, we use Microsoft Azure's Multi-Factor Authenticator mechanism, requiring not only the correct password but also biometric verification via an app, significantly increasing the security of our front-end member website. Additionally, we use Microsoft Azure VPN encrypted channels to connect to the EDA tool usage environment, similar to how we use VPNs to remotely control it from home, ensuring that your data is protected from attacks and theft on the Internet. The entire Microsoft-provided cloud infrastructure and data centers are ISO certified and comply with multiple related data security certifications and legal requirements, offering a safe environment for development.

What are the other advantages of the subscription-based cloud EDA tool platform sevice?

The subscription-based cloud EDA tool platform service allows users to immediately use EDA tools through a browser connected to the cloud server after subscribing, without the need for complex installation and configuration. This convenience not only makes usage easier but also reduces maintenance costs for workstations. Without being limited by location, as long as there is a standard computer and a stable internet connection, users can easily operate the EZ-BIST tool and quickly create optimized MBIST circuits, shortening the time for IC design.

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Episode 12: Algorithms specifically designed for different faults - Part 1

iSTART-TEK has a professional tool for BIST algorithms. It can produce different algorithms even though the complexity might be very high. Could you help to introduce the tool to us?

Currently, “METHOD FOR GENERATINGAN MEMORY BUILT-IN SELF-TEST ALGORITHM CIRCUIT” has already obtained the U.S. patent certification, and User Defined Algorithm platform, UDA, uses the format of this patent. It’s possible to remove the repeated elements, and what’s more, you can edit the algorithm and define the address of memory in a file by yourself, which can shortening the test time. The key point is that it’s very intuitive to use. No matter how many reads or writes you want to use in your algorithm, just directly write them onto the file and turn on the corresponding tool settings. Even if you want an algorithm with a complexity of 68N, or even much higher, it can be easily created. If you want to know more detailed like how to setup, feel free to contact our technical support engineers.

What is a fault? And how is it generated?

In the circuits of Memory, due to manufacturing processes, there might be occurrences like necking or bridging of circuits, or with time, there might be IR-drop leading to circuit breaks. All these are collectively known as faults.

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Episode 13: Algorithms specifically designed for different faults - Part 2

What algorithms does iSTART-TEK have to detect the locations of these faults?

The algorithms at iSTART-TEK are configurable, meaning they can be customized and merged, ranging from the basic March algorithm to highly complex ones, like our extremely intricate algorithm Polaris. By integrating these with the Diagnosis function in our EDA tools, it becomes easy to locate the origins of these faults. While finding the location is important, what's even better is, from which different wafers are collected, identifying which areas have more faults. This information can be fed back to the wafer fabrication plants, thereby improving the overall yield of the wafers.

What types of faults are there?

Here we introduce several common types of faults, such as SAF, which stands for Stuck-At-Fault. This means that the affected cell in this error will always remain at 0 or 1 and won't be able to obtain any other values. Next is TF, which is a Transition-Induced Fault, indicating that this cell cannot undergo a transition. RDF is caused by a state change due to a Read operation, while DRDF is also caused by a state change due to a Read operation, but the read value remains correct. WDF occurs when the cell should undergo a transition but doesn't. IRF occurs when there is no change in state during a Read operation, but the read value is incorrect. Additionally, there are NPSF, which are neighborhood pattern-sensitive faults, including ANPSF, where neighboring cells transitioning can affect the base cell.

DRF, which stands for Data Retention Fault in dynamic random access memory, is caused by very high resistive-open defects affecting the refresh loop of the core unit. Lower resistance values can also lead to DRFs that are difficult to detect. There are many other types of faults, such as Coupling Faults, SCFs, DCF, NPSF, SNPSF, ANPSF like this. If you want to learn more, you can contact the technical team at iSTART-TEK for further information.

Watch the Video

Episode 14: EZ-Safety & EZ-TEC

What's the scoop with EZ-Safety?

EZ-Safety SRAM IP is our charm for automotive chips, tailored to meet the ISO 26262 standards, making chip design wizards more adept at conjuring car-friendly chips. It cozies up with your existing memory test circuits, taking a snapshot of crucial memory before it runs its diagnostic spells. If the memory's read-write spells are spot-on, it restores the data; if not, it alerts the chip's mastermind. Plus, its block-building architecture makes it a breeze to embed into SoC castles. Just link it to key memories, and voilà, data backup, testing, and restoration are done in a snap.

And what about EZ-TEC?

EZ-TEC SRAM IP, sharing space with your memory test circuits, springs from our U.S. patented "METHOD FOR GENERATING AN MEMORY BUILT-IN SELF-TEST ALGORITHM CIRCUIT." It breaks down memory test algorithms into elements, allowing you to tailor any test algorithm by rearranging these elements. After BIST spells reveal memory flaws, you can remix elements to cast a new test spell, retesting crucial memories to lower DPPM and boost chip quality. Like EZ-Safety, EZ-TEC uses a block-building architecture for easy use.

What makes these IPs stand out?

EZ-Safety SRAM IP not only aligns with ISO 26262, running independently from any MBIST structure but also ensures the integrity of crucial memories with its intuitive design, making embedding and integration a walk in the park. Similarly, EZ-TEC operates independently, enabling the design of optimal circuits through a modular approach and allowing for effective retesting of key memory flaws, thus minimizing DPPM.

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Episode 15: eFlash BIST IP

About eFlash BIST IP

eFlash BIST provides test items that meet automotive electronic requirements, encompassing all the test items required by vendors. Due to eFlash has been using to store the initializing data of ROM, it will be important to cruise safety. All test items of eFlash BIST IP can be turned on and off individually. Additionally, it offers the ability to adjust time parameters on the machine, repair functions, and enhance the yield of the eFlash macro. It also provides a diagnostic feature, pass or fail of diagnosing of fault information, and offers a flexible interface, which is quite convenient for inputting test vectors into the machine.

The POT of the eFlash BIST IP

The POT (Power_On Test) so far of the eFlash BIST IP provides a life cycle test for eFlash after power-on, ensuring that eFlash can be used normally after each startup. The result of the diagnosis, like pass or fail, is indicated through MGO and the finishing of whole test or not will be indicated by MRD signal.

The advantages of the eFlash BIST IP

The eFlash BIST IP not only meets the test items of ISO 26262 for automotive electronics but also all the test items required by suppliers. All test items can be individually activated and deactivated, and it allows for the adjustment of time parameters on the machine, enhancing the yield of the eFlash macro. Additionally, it provides a diagnostic function that can quickly identify erroneous information; lastly, the eFlash BIST IP offers a flexible interface for easy input of test vectors into the machine.

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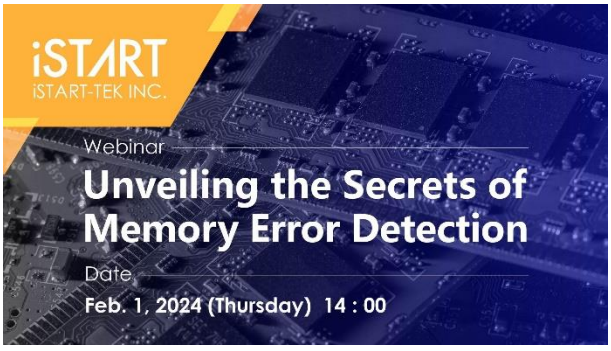
iSTART Webinar : Unveiling the Secrets of Memory Error Detection



On Fab. 1st, 2024, we held a webinar focusing on various aspects of memory error detection, exploring the types of memory errors, testing algorithms, and the customized memory testing and repair solutions provided by iSTART-TEK.