iSTART iReport

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iSTART-TEK INC.

News

iSTART Class

Events

iSTART-TEK Certified with ISO 26262 TCL1

iSTART-TEK's have been certified with Tool Confidence Level 1 (TCL1) under the "ISO 26262:2018 Road Vehicles — Functional Safety" standard. This has also been evaluated and approved by DEKRA, an internationally recognized third-party testing and validation organization. ISO 26262 is an international standard for ensuring the safe operation of automotive systems. Achieving ISO 26262 TCL1 certification signifies that iSTART-TEK's EDA tools have received the highest level of international recognition.

The Repair, POT (Power_On Test), UDA (User-Defined Algorithm) and ECC (Error-Correcting-Code) functions fully comply with the stringent requirements of ISO 26262 ASIL (Automotive Safety Integrity Level) D, assisting customers in achieving the ASIL certification. iSTART-TEK's achievement of ISO 26262 TCL1 certification demonstrates the company's expertise in the field of automotive functional safety with its EDA tools.

Learn More

ISO 26262

ISO 26262 Tool Confidence Level 1 (TCL1)

(1) **Certificate**

(2) Number of Certificate: **ZP/C032/24**

(3) Subject of Certification: **START Tool for the use in Safety related Developments**

(4) Company: **iSTART-TEK INC.**

(5) Address: **30288 7F.-5, No. 6, Taiyuan 1st Street, Zhubei City, Hsinchu County, Taiwan (R.O.C)**

(6) N/A

(7) The certification body of DEKRA Testing and Certification GmbH certifies that the FSMS and their related processes of the Company referred in section (4) have been found to comply with the essential requirements pursuant to the standard(s) referred in section (8). The assessment results are summarized in the assessment report FSAR_08042024_V1_iSTART.

(8) The requirements are assured by compliance with the following standard(s):

ISO 26262-2:2018, ISO 26262-5:2018, ISO 26262-6:2018, ISO 26262-8:2018, ISO 26262-11:2018

(9) This certificate only relates to the subject of certification in accordance with the mentioned standard(s).

(10) Assessment Report(s)

FSAR_08042024_V1_iSTART dd. 2024-05-17

(11) This certificate is valid until 2029-06-09

DEKRA Testing and Certification GmbH
Bochum, 2024-06-10

Managing Director

Page 1 of 1 of ZP/C032/24
This certificate may only be published in its entirety and without any change.
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Memory Testing and Repair IPs Best Suited for Chiplet

Chip design becomes more difficult, and its workflow becomes complicated as semiconductor processes evolve. Under this trend, chiplet technology that can simplify chip design and manufacturing workflow, efficiently improve chip performance, and sustains Moore's Law is highly anticipated in the industry.

From a system design perspective, various hardware functions can be divided into chiplets, which can be manufactured using different IC process nodes and even non-silicon materials to meet the demands for low cost and high performance. According to Omdia's projections, the global chiplet market size is expected to reach $5.8 billion by 2024 and is projected to exceed $57 billion by 2035.

Chiplet technology involves disaggregating functions originally integrated into SoCs. Challenges such as designing interconnect architectures between multiple chiplets, addressing heat dissipation issues after chip stacking, and managing aspects like chip testing, software integration, and responsibility allocation are common in chiplet endeavors. Addressing these challenges requires corresponding design processes, methodologies, and tool support.

The memory testing and repair IPs introduced by iSTART-TEK, including EZ-Safety, EZ-TEC, and EZ-Monitor, can all be applied in chiplet technology.

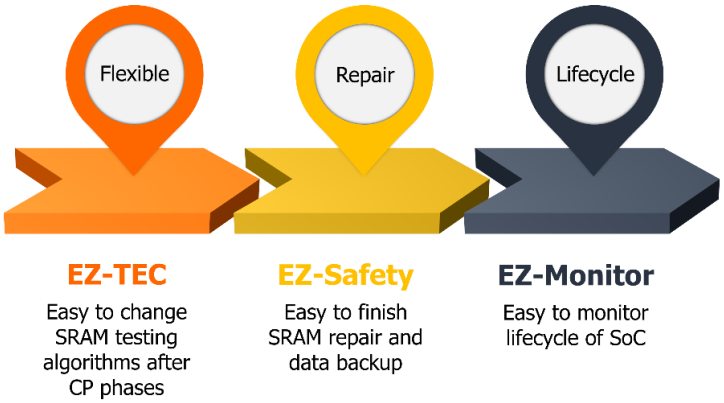
EZ-Safety improves memory testing efficiency by extracting essential signals required during memory testing. It automatically backs up designated memory information and is not restricted to testing only in the test mode, thereby enhancing overall security. Additionally, EZ-Safety is easy and intuitive to embed and integrate, providing real-time and flexible memory testing capabilities.

EZ-TEC is also easy to embed and integrate into IP designs. It dynamically adjusts memory testing algorithms, allowing designers to customize element definitions of the testing algorithm according to the specific requirements of individual chiplets, in addition to the commonly used algorithms. EZ-TEC is the world's first technology to modify memory testing algorithms after chip mass production, thereby improving chip yield.

EZ-Monitor ensures the memory lifecycle within the chip, and effectively monitor the lifecycle of each individual chiplet.

As semiconductor fabrication approaches known physical limits, the continuous enhancement of processor performance necessitates the adoption of chiplet and heterogeneous integration technologies. These approaches are regarded as primary solutions for sustaining Moore's Law. The memory testing and repair IPs provided by iSTART-TEK are well-suited for chiplet implementations, offering an effective means to improve the yield of individual chiplets.

Learn More



iSTART Class

Ep 1: BIST & BISR

Ep 2: iSTART-TEK Achieves ISO 9001:2015 Certification

Ep 3: Testing Algorithms

Ep 4: EZ-Debug

Ep 5: iSTART-TEK Tech Support Services

Ep 6: START & EZ-BIST

Ep 7: ITE & Rafael Micro Customer Interview

Ep 8: Specific Functions for Auto & HPC

Ep 9: EZ-Safety & EZ-TEC (Preview)

Ep 10: EZ-Debug & Diagnosis

Ep 11: iSTART-Cloud

Ep 12: Algorithms Designed for Various Faults – Part 1

Ep 13: Algorithms Designed for Various Faults – Part 2

Ep 14: EZ-Safety & EZ-TEC (Detailed)

Ep 15: EZ-eFlash BIST IP

Ep 16: Algorithms for Detecting Memory Errors Under High Temperature

Ep 17: Memory Testing Algorithms for CIM Applications

Ep 18: iSTART-TEK Launches ASIC Design Services

Ep 19: Customized IP Compliant with Auto Electronics Standards

Ep 20: EDA Tools Compliant with Auto Electronics Standards – Part 1

Ep 21: EDA Tools Compliant with Auto Electronics Standards – Part 2

Ep 22: The Importance of Using Licensed EDA software

Ep 23: Make MBIST Much Easier with EZ-TEC IP

Webinar

Highlights:

- Why Choose UDA? – The world's unique custom SRAM testing algorithm platform
- What Does UDA Offer? – Customizable algorithms, GUI mode, and element reconfiguration
- How to Use UDA? – Sign up now to learn more !

Register at https://jinshuju.net/f/TLhoMR

Highlights:

- Why Choose EZ-TEC? – The most flexible SRAM testing IP that meets all your testing requirements
- EZ-TEC's Unique Features? – Diverse interfaces, flexible element reconfiguration, and MBIST architecture
- Experience EZ-TEC IP Now

Register at https://jinshuju.net/f/QQQ4NT