iSTART iReport

iSTART TEK INC.

iSTART-TEK Introduces EZ-BIST Lite for MCU Chip Customers

Microcontrollers (MCUs) play a critical role in the global semiconductor industry, including applications in consumer electronics, automotive electronics, IoT, and industrial use. To assist MCU chip suppliers in expediting memory test circuit development, iSTART-TEK has launched EZ-BIST Lite, a memory test circuit development environment tailored for MCU chips. EZ-BIST Lite features a user-friendly graphical user interface (GUI) to facilitate the experience for first-time users in memory test circuit development (Figure 1).

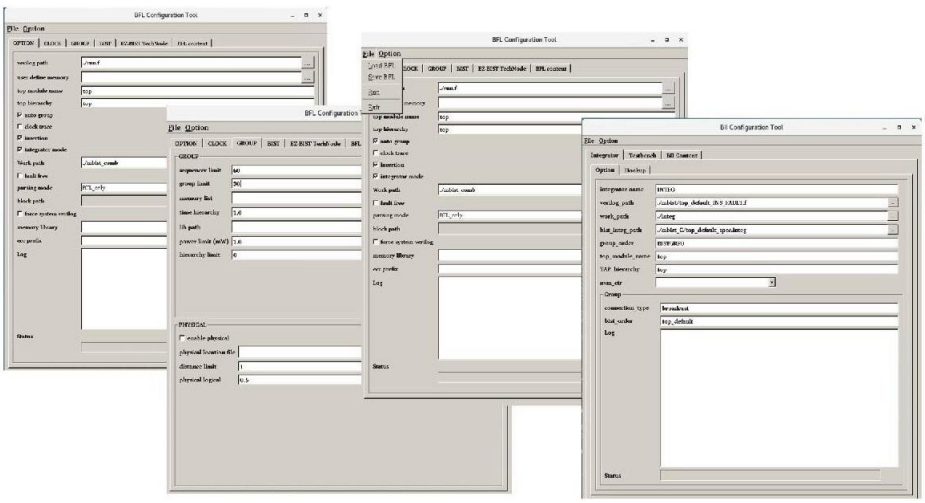

Figure 1

Additionally, EZ-BIST Lite provides an interface for selecting diverse memory testing algorithms, enabling first-time users in memory test circuit development to easily choose the appropriate algorithms (Figure 2).

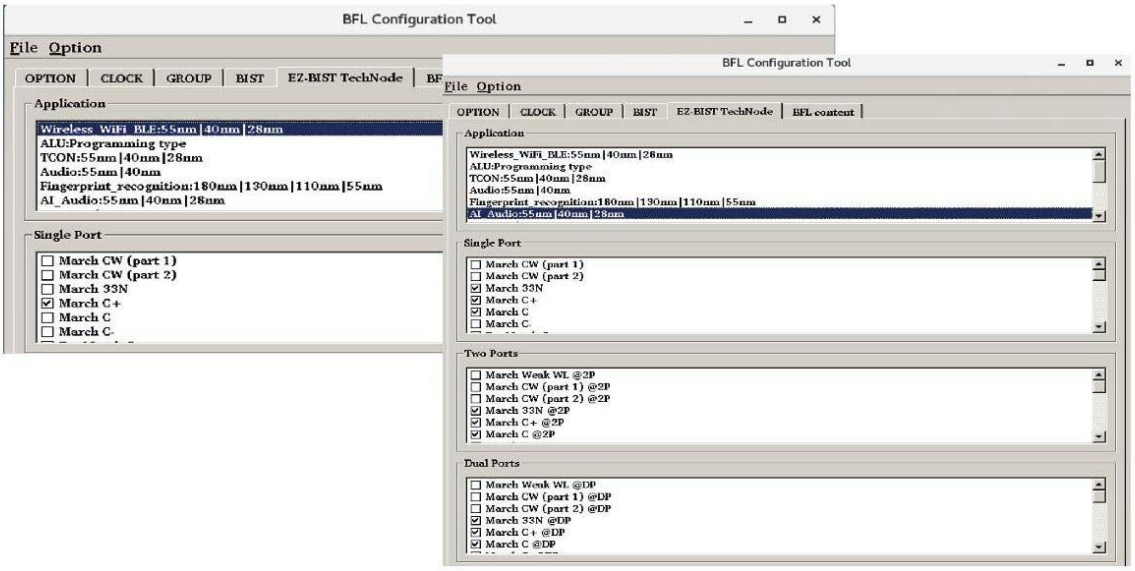

Figure 2

iSTART-TEK is Asia's only EDA tool and IP provider that specializes in memory testing and repair circuit development. To enable more MCU-relevant chip suppliers to access customized memory EDA tools, iSTART-TEK has introduced EZ-BIST Lite, specifically designed for the MCU chip suppliers. EZ-BIST Lite is license fee-free, significantly reducing the cost for MCU customers in using memory test circuit development environments. Its user-friendly GUI interface ensures easy adoption, effectively lowering the technical barriers during tool implementation. In the future, iSTART-TEK will charge a royalty fee once the customer's chip that utilizes EZ-BIST Lite reaches the mass production stage.

If you are interested in using EZ-BIST Lite, please visit here to fill out the application form. iSTART-TEK will provide the download link after review.

iSTART-TEK aims to serve more MCU chip suppliers through EZ-BIST Lite, assisting them in reducing chip design costs and DPPM (Defective Parts Per Million) as well as enhancing chip quality.

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iSTART-TEK's Customized eFlash Test and Repair IPs Adopted by Chinese Automotive SoC Suppliers

As the global automotive industry moves towards electrification and intelligence, the demand for automotive SoCs has significantly increased due to continuous advancements in automotive electronic technology. According to "IC Insights", the automotive SoC market is projected to account for 9.9% of the overall IC market value in 2026, with a compound annual growth rate of 13.4% expected from 2021 to 2026. It is anticipated to become the fastest-growing semiconductor application market, driven by the specification advancements in various ICs such as sensors and analog ICs. The growth momentum is also fueled by the continuous improvement of electric and energy vehicles.

To ensure the proper functioning of automotive electronic chips under various complex scenarios while ensuring driving and passenger safety, iSTART-TEK has developed the configurable eFlash IP testing and repair circuit development environment, EZ-NBIST (Non-Volatile Memory Built-In Self-Test). EZ-NBIST is a customized EDA tool for eFlash testing and repair circuit development, accessible through a user-friendly GUI (Graphical User Interface). It significantly reduces eFlash testing time and lowers testing costs.

The customized eFlash testing and repair IPs provided by iSTART-TEK is generated using their EDA tools, EZ-NBIST. Users can select their preferred test interface and eFlash size through EZ-NBIST. Based on the users' configurations, EZ-NBIST automatically generates the testing and repair circuits for eFlash. Additionally, users can integrate the customized eFlash testing and repair IP into their SoCs.

The benefits of using customized eFlash testing and repair IPs are as follows:

1. It can save time on learning how to use EDA tools.
2. The configurable test options lead to cost reduction in eFlash testing.

iSTART-TEK's EZ-NBIST has been adopted by Chinese semiconductor manufacturers for generating eFlash test and repair circuits. Additionally, the customized eFlash test and repair IPs have also been adopted by Chinese automotive SoC developers. Whether users choose EZ-NBIST or the customized eFlash test and repair IPs, they can configure the test options through a configurable interface, significantly reducing eFlash testing costs.

Using EDA tools or IPs has become an essential part of SoC design. iSTART-TEK's EZ-NBIST and customized eFlash test and repair IPs can fully meet customers' needs in saving chip testing costs, effectively reducing chip testing expenses, and enhancing chip competitiveness.

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iSTART-TEK's Customized IP Adopted by Automotive SoC Suppliers

With the rapid development of the semiconductor industry, emerging applications such as automotive electronics, artificial intelligence, Internet of Things, and cloud computing have increasingly higher demands for chip functionality and performance. Coupled with the continuous advancement of semiconductor processes, chip structures and the complexity of their functionalities have increased, resulting in greater challenges in chip design and an increased demand for Intellectual Property (IP).

iSTART-TEK specializes in memory testing and repair solutions as well as customized IP services, which provide customers with highly flexible and differentiated solutions. Additionally, iSTART-TEK 's customized IPs enable IC design companies to tailor memory testing and repair functionalities specifically to chip performance, thus enhancing product lifespan and competitiveness.

iSTART-TEK's customized IPs have been successfully adopted by automotive SoC suppliers. The main reasons include: 1. Customized IPs can help reduce the time required to learn EDA tools. 2. iSTART-TEK can tailor customized IPs with specific functionalities based on the specific characteristics and requirements of customers' chips. The customized functionalities include Power On Test (POT) for automotive SoCs and Circuit Self Verification (CSV) for memory testing circuits, which can be designed to meet the safety regulations and requirements of automotive applications.

As global automotive market moves towards electric vehicles, automotive manufacturers are competing to develop safer, more comfortable, and more convenient high-tech vehicles. iSTART-TEK 's customized IPs have already been successfully mass-produced for automotive electronic chip suppliers, including applications in driving safety inspection, car screens, and car charging chips. In the precision-driven semiconductor industry, using IP is indispensable for SoC design. iSTART-TEK 's customized IPs can fully meet customers' customized needs in various functions, significantly reducing chip design time. This allows the company to seize market opportunities and enhance its competitiveness in the highly specialized semiconductor industry.

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Rafael Micro and iSTART-TEK Collaborate to Launch a Multi-Channel Mobile TV Wireless Receiver with Built-in Memory Self-Repairing Function

In recent years, the mobile TV market for cars has been growing rapidly. This emerging market is driven by various factors, including increasing demand for in-car entertainment, real-time news and information collection, advancements in mobile broadcasting technology, and rapidly evolving in-car communication infrastructure. Due to its compatibility with various in-car devices and high-resolution capabilities, consumers' interest in mobile TV for cars is rapidly increasing.

Rafael Micro has launched a multi-channel mobile TV wireless receiver chip for its customers. It is a solution that includes multiple RF tuners and an integrated digital modulator. Each tuner can be configured independently, and each customized tuner has an independent output that supports wireless signals such as VHF and UHF frequency bands. For example, ISDB-T has the advantages of high-quality audio and video and scalability, which is why it is frequently used in the automotive TV decoding market in many countries and regions.

RF TV decoding chips with multiple outputs require the integration of a large number of multi-channel RF and analog circuits, as well as a highly complex digital decoding design. The SRAM memory modules used in the pipelined operation structure are also numerous. To ensure that such a large amount of memory can maintain the highest yield in new manufacturing processes, iSTART-TEK provides memory testing and repair solutions to IC developers to address production pain points in the industry. This further improves yield, reduces defect rates and testing time, and ensures maximum profit margins for customers.

"The testing and verification of wireless SoCs are the most difficult parts in the entire design process, especially they need to comply with automotive regulations," said Mr. Ken Li, co-President of Rafael Micro, "The overall performance, reliability, defect rate, immunity to interference, compatibility, and production testing of RF-related components are all critical factors that need to be carefully considered."

As Asia's only provider specializing in memory testing and repair solutions, iSTART-TEK exclusively customized design services, and its main products include EDA tools and customized IPs.

Rafael Micro has adopted START™ v3, iSTART-TEK's EDA tool for customized memory testing and repair, on their RT58 series multi-channel mobile TV wireless receiver chips. START™ v3 has built-in self-testing features that can generate high-quality wireless SoCs. This customized EDA tool contains high-complexity testing algorithms and high-efficiency repair technologies, helping chip developers reduce design costs, shorten design time and increase chip yield.

About Rafael Microelectronics, Inc.

Rafael Micro is a fabless IC design company that focuses on high-end broadband RF technology and continues to extend its core technology to digital and high-speed optical communications. Its products include TV RF IC, STB RF IC, modulator chip, satellite broadcast LNB, optical communication IC and BLE 5.1/5.2 and Sub-GHz IoT communication chips. Rafael Micro's product lines performance, quality and engineering services quality have been highly recognized by customers.

For more information, please visit the website: http://www.rafaelmicro.com/

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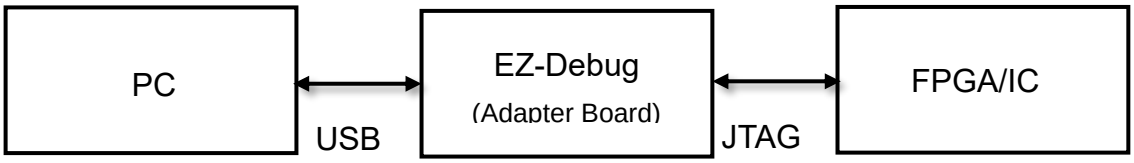
Highly Cost-effective Memory Debugging Tool: EZ-Debug

In the rapidly evolving IC industry, ensuring that ICs conform to design specifications and functionalities is indispensable and vital in the development and manufacturing processes. Thus, the IC industry extensively adopts automatic test equipment (ATE) to conduct testing tasks. However, in the past, dealing with small batches or non-mass-produced chip testing often required the use of ATE machines, which came with additional costs and lengthy testing times.

Recently, iSTART-TEK has developed a JTAG-to-USB debugging tool called EZ-Debug, based on the PC platform. This tool enables fast and efficient testing for non-mass-produced chips and chips under development. It not only reduces costs associated with ATE testing but also provides real-time insight into debugging results.

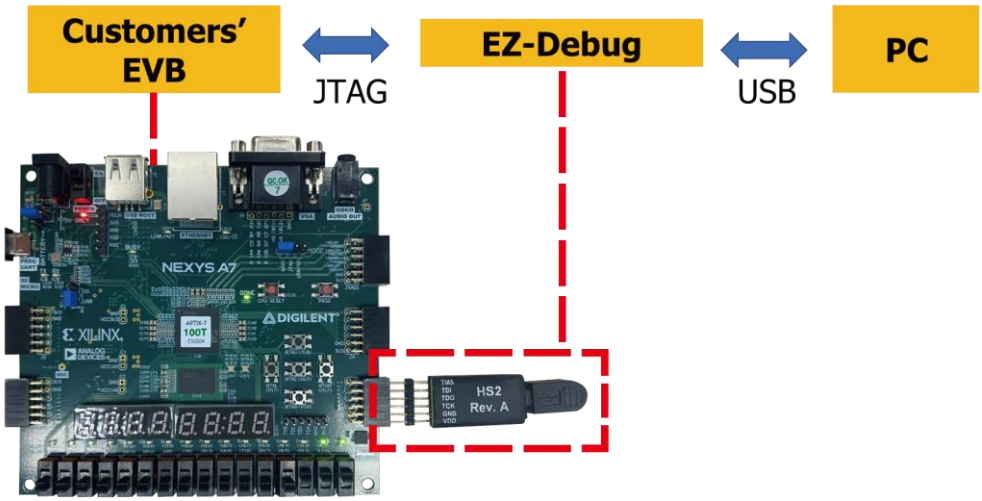
I. EZ-Debug Architecture

EZ-Debug enables fast and convenient debugging. The main communication between the PC and the FPGA/IC board is achieved through an adapter board. The specifications of the adapter board and the tool's overall architecture are illustrated in the diagram below. The PC is connected to the adapter board via the USB, and the adapter board, in conjunction with the tool, converts signals into the JTAG format before transmitting them to the FPGA/IC board for debugging.



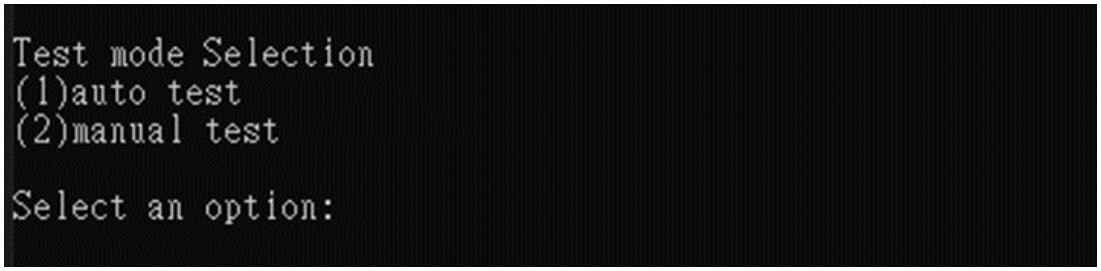
Architecture Diagram

The figure below shows the actual usage. In the red box is the adapter board, and on the right side of the adapter board is the FPGA. The left side is connected to the PC. This FPGA is utilized to simulate non-production chips and chips under development.

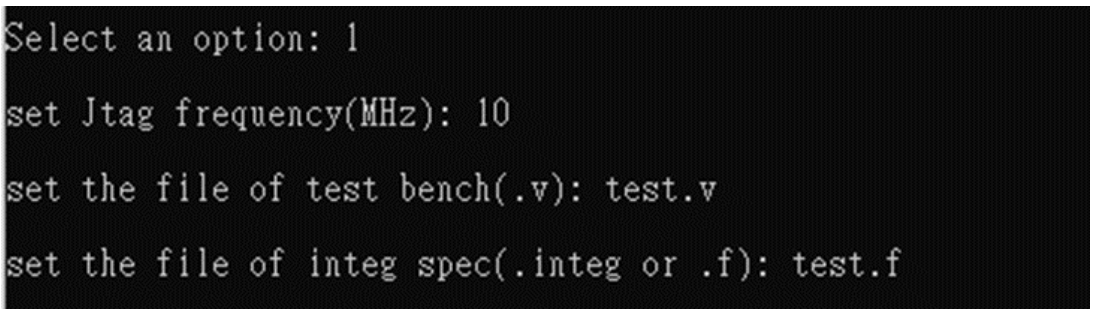


II. Practical Usage of EZ-Debug

After installing EZ-Debug and the driver of the adapter board, we can start using the debugging tool. EZ-Debug provides two types of testing modes: (1) auto test and (2) manual test.



1. EZ-Debug Testing Mode – Auto Test



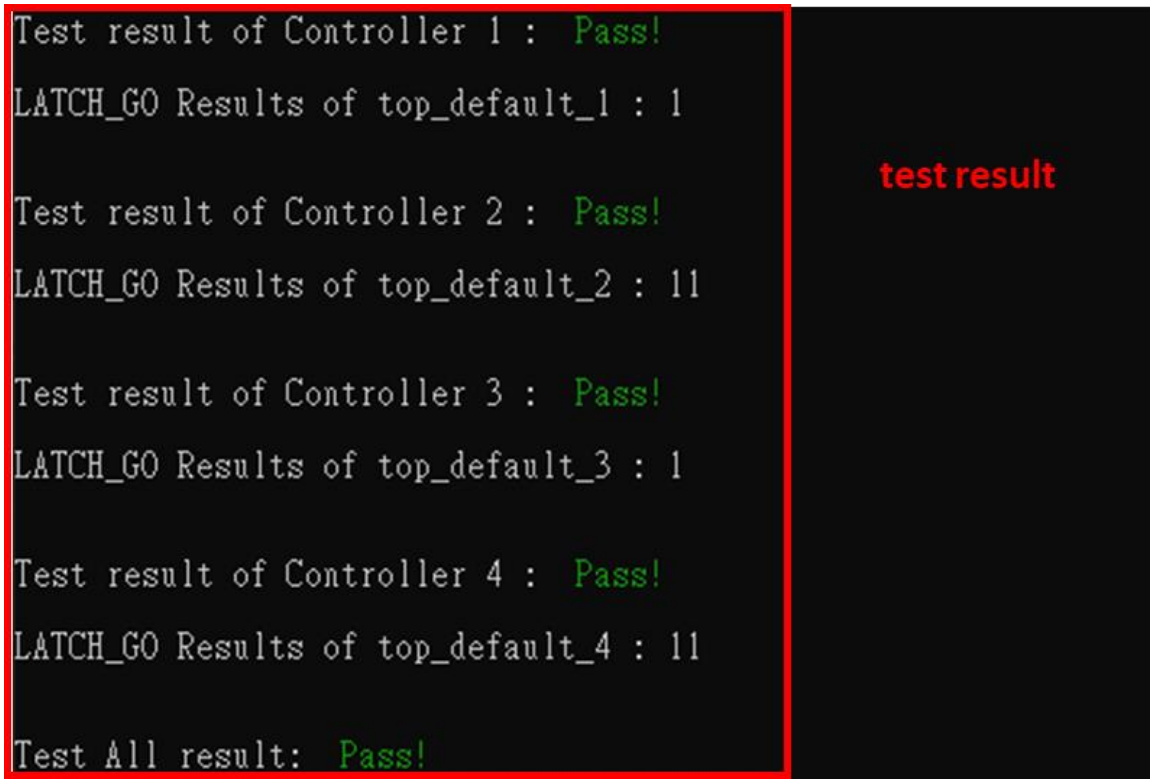
We need to set the JTAG frequency, along with the testbench file and integ spec file generated by START™ v3. After configuration, EZ-Debug will conduct BIST testing automatically.

- JTAG Frequency: This refers to the frequency at which JTAG operates on the FPGA/IC.
- Testbench File: This is the file generated by START™ v3 during BII for simulation (e.g., integ_tb.v).
- Integration Specification File: This is the file generated by START™ v3 during BFL for BII integration (e.g., [ctr_name]_spec.integ).

During auto test, EZ-Debug will conduct BIST testing for every controller in the design and display the testing results on the screen. If the inserted BIST circuits support the LATCH_GO function, EZ-Debug will also display the LATCH_GO results.

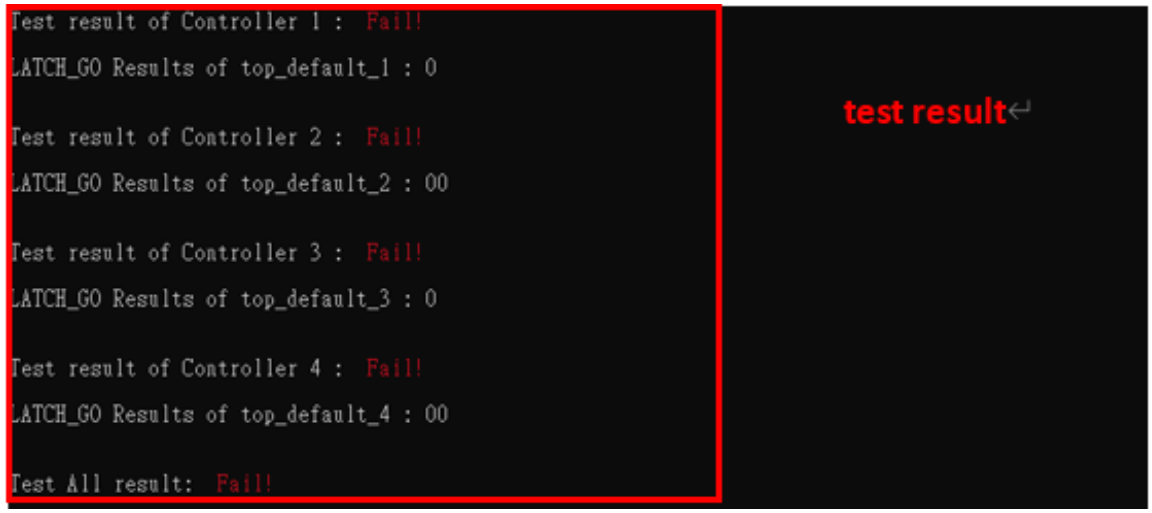
If the testing result is PASS, it will show "Test Pass!" and the LATCH_GO result is "1".

[Test Pass]



If the test result is FAIL, it will display "Test Fail!" and the LATCH_GO result will be "0". If the inserted BIST circuits support the Diagnostic function, EZ-Debug will perform diagnostic testing and show the information of completed diagnostic testing on the screen.

[Test Fail]




```
------------ Start to Diagnosis Memory of top_default_1 ----------------
------------ Memory of top_default_1 SEQ 1 GRP 1 MEB 1 Fail! ---------------
------------Diagnosis Information---------------
Algorithm :      1
Sequencer ID :   1
Group ID :       1
Element :        001
Operation :      0011
Faulty Address : 0000000001
Faulty Bits :    00000000010000000000000000000000
-------------------------------------------------

------------ Memory of top_default_1 SEQ 1 GRP 1 MEB 1 Fail! ---------------
------------Diagnosis Information---------------
Algorithm :      1
Sequencer ID :   1
Group ID :       1
Element :        001
Operation :      1000
Faulty Address : 0000000001
Faulty Bits :    00000000010000000000000000000000
-------------------------------------------------

------------ Memory of top_default_1 SEQ 1 GRP 1 MEB 1 Fail! ---------------
------------Diagnosis Information---------------
Algorithm :      1
Sequencer ID :   1
Group ID :       1
Element :        010
Operation :      0011
Faulty Address : 0000000001
Faulty Bits :    00000000010000000000000000000000
-------------------------------------------------
```

2. EZ-Debug Testing Mode – Manual Test

   Firstly, refer to the "bist_testing" task in the INTEG testbench that has completed integration. In this task, we can find the CMD_DATA information as shown in the diagram below. Simply follow the information in the diagram to set the input binary value for sending commands using the JTAG's TDI, and then we can start testing.

```
top_default_CMD_DATA = {top_default_DIAG, top_default_ALG,
                        top_default_SEQ_ID, top_default_GRP_ID,
                        top_default_MEB_ID, top_default_MEN};
```

- [ctr_name]_DIAG: It determines whether to execute Diagnosis. Set to 1 to enable.
- [ctr_name]_ALG: When the algorithm_selection option is enabled in the BFL settings, the testbench generates the Controller_name_ALG command to control the desired testing algorithm.
- [ctr_name]_SEQ_ID, Controller_name_GRP_ID, Controller_name_MEB_ID: These are used to specify the ID of the memory being tested.
- [ctr_name]_MEN: It is the command to enable Controller BIST. Set to 1 to enable.

JTAG's TDO will generate capture_commad, which can be interpreted by referring to the test_result signal arrangement in the INTEG testbench.

```
{top_default_MGO, top_default_MRD,
top_default_SRD, top_default_LATCH_GO} = top_default_test_result;
```

Signal Interpretation:

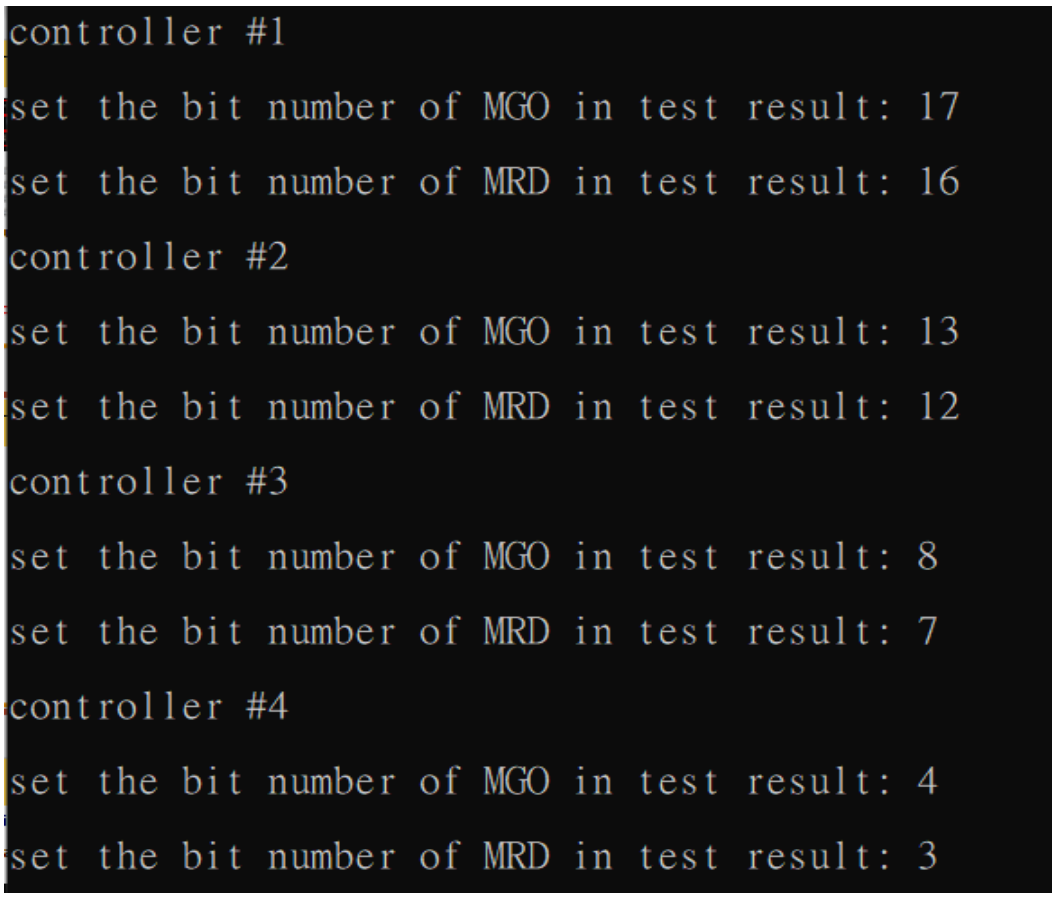
- [ctr_name]_MGO: It is the BIST testing result. When the testing fails, it is 0.
- [ctr_name]_MRD: It is 1 when the BIST testing is completed.
- [ctr_name]_SRD: When the Diagnosis Data is ready, it will be 1, indicating that capturing Diagnosis Data can proceed.
- [ctr_name]_LATCH_GO: The width of this signal is determined by the memory quantity in the meminfo file generated by START. When every signal of LATCH_GO turns from 1 to 0, it means that this memory testing fails.

When using the tool, input the number of controllers, the test commands, the length of capture result, and the bit number of MGO/MGD. EZ-Debug will then conduct the testing and display the row-data of the test results on the screen.

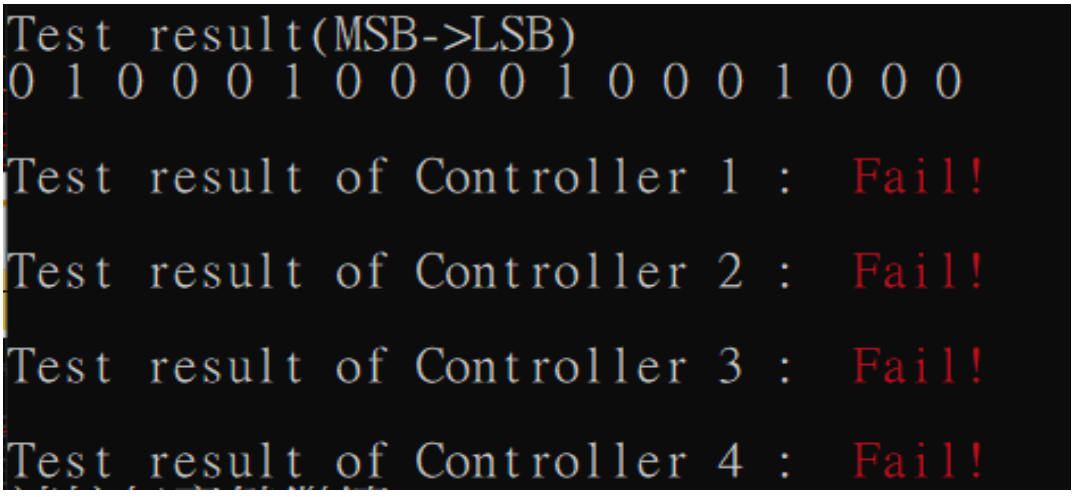
[Input the testing commands]

```
Select test:
(1)bist test
(2)diagnosis test

Select an option: 1

set the number of controller: 4
set the cmd data(MSB->LSB): 00110100110010011010011001
set the size of capture data: 18
```

[Input the MGO/MRD bit number]



[Testing results]



Authored by Erick Chang, Manager at iSTART-TEK INC.

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Events

iSTART-TEK Design Workshop (iDW)

Date: August 2 (Wed), 2023
Time: 14:00-17:00
Location: Sheraton Hsinchu Hotel

iSTART-TEK Design Workshop (iDW) has successfully concluded! During the event, we shared comprehensive memory testing and repair solutions along with various innovative technologies. We also highlighted our cost-effective chip memory diagnostic tools and EDA tool cloud service.

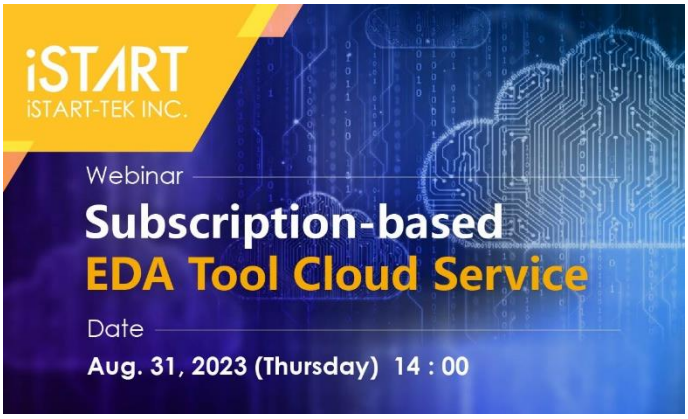
iSTART-TEK Technical Forum

Hsinchu Venue
Date: October 19 (Thu), 2023
Time: 14:00-17:00
Location: 3F, Sheraton Hsinchu Hotel
Shanghai Venue
Date: October 26, 2023 (Thursday)
Time: 14:00-17:00
Location: 2F, Evergreen Laurel Hotel (Shanghai)

2023 iSTART-TEK Technical Forum has successfully concluded at both Hsinchu and Shanghai! We extend our heartfelt gratitude to all distinguished guests for your enthusiastic participation. iSTART-TEK will continue to strive for excellence, optimizing technology development and innovation to provide our customers with more solutions.

Events

DVCon Taiwan



SaaS EDA Tool Cloud Service

iSTART Class | EZ-Debug

iSTART Class | Testing Algorithms

iSTART Class | BIST & BISR

YEESTOR Honored with the 2023 "China Chip" Outstanding Market Performance Product Award

On September 20th, the results of the 18th "China Chip" Award were announced at the 2023 Henqin Zhuhai Macao IC Industry Promotion Summit. With outstanding product capabilities and impressive market performance, YEESTOR Microelectronics (YEESTOR) stood out among numerous participating products and was honored with the 2023 "China Chip" Outstanding Market Performance Product Award for its "YS9082XX" series industrial and laptop solid-state hard drive storage control chips.

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Unicomsemi Honored with the 2023 "China Chip" Emerging Product Award

Congratulations to Unicomsemi, a company specializing in the design of intelligent charging and smart grid communication chips! Their HomePlug® GreenPHY chips MSE1021+MSEX24-i and MSE1022+MSEX25-i, have been honored with the "China Chip" Emerging Product Award at the 18th "China Chip" Award Ceremony organized by China Center for Information Industry Development. These products stood out after facing fierce competition in the evaluation process and were recognized with the "China Chip" Emerging Product Award.

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YEESTOR Winning "Outstanding Controller Service Award" at GMIF 2023

At the "Global Memory Industry Innovation Forum (GMIF) 2023, YEESTOR was honored with the "Outstanding Controller Service Award". This recognition signifies a high level of acknowledgment for YEESTOR's years of dedication to research and development of memory control chip technology as well as their capabilities in providing high-quality services.

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YEESTOR's Automotive-Grade eMMC Chips Included in 2023 Catalog

Congratulations to iSTART-TEK's customer, YEESTOR Microelectronics Co., Ltd, for the successful inclusion of its multiple automotive-grade eMMC storage chips in the "Domestic Automotive-Grade Chip Reliability Classification Catalog (2023)"!

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CR Micro's Latest Release of Its New Generation 0.15μm 40V BCD Process Platform

CSMC Technologies Fab2 Co., Ltd., a subsidiary of China Resources Microelectronics Limited (CR Micro), announced in August 2023 the official release of their latest 0.15μm 40V BCD process platform. This advanced process platform focuses on high-power power management chips and electric machine control chips, catering to applications such as fully integrated motor drivers, high-performance DC-DC converters, and other PMIC applications.

CSMC's new generation 0.15μm 40V BCD process platform has undergone technological enhancements to meet the application requirements for medium to high-power electronic products. The performance of power transistors in this new BCD process has been significant improved, with a reduction of approximately 20% in the FOM and enhanced EAS capability along with ESD protection features. Furthermore, this new generation process platform has significantly improved isolation performance, reduced substrate leakage current, and greater latch-up suppression capabilities in power transistors.

This process platform offers a rich variety of device options, including Depletion MOS, Zener diodes, Schottky diodes, JFETs, MIM, and MOM, as well as IP options such as SRAM, e-FUSE, and MTP. Compared to the previous generation BCD process, the new generation process platform provides improved cost-effectiveness. The number of mask layers for both the pure 5V base process and the 1.8V+5V process has been reduced, resulting in a significant reduction in overall chip production costs.

In the future, CSMC will continue to develop and upgrade its analog process technology, contributing to the development of a reliable semiconductor ecosystem.

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