iSTART iReport

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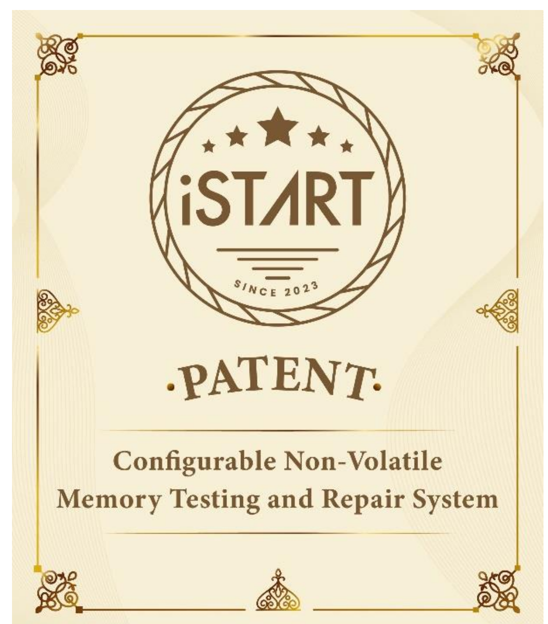
Configurable Non-Volatile Memory Testing and Repair System

iSTART-TEK has successfully obtained a new patent certificate for its "Configurable Non-Volatile Memory Testing and Repair System". This patent further solidifies iSTART-TEK's leading position in the field of memory testing, repair, and the EDA tool market.



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Event

VIP Spring Tea Party

Date: March 29 (Wednesday)
Time: 09:00-16:30
Location: Evergreen Laurel Hotel (Shanghai)

The iSTART-TEK 2023 VIP Spring Tea Party has successfully concluded. This year's event was held at the Evergreen Laurel Hotel Shanghai, with the presence of numerous distinguished guests. During the event, iSTART-TEK presented solutions for automotive electronic chips and showcased the most cost-effective memory debugging tools. We also invited several eco-system partners to share their insights on stage. We would like to express our gratitude to all the esteemed guests for their participation and support.

CWGCE 2023

Date: April 26-28, 2023
Time: 09:00-16:30
Venue: Chengdu Century City New International Convention & Exhibition Center

Global Semiconductor Industry Expo Chongqing (GSIE) 2023

Date: May 10-12, 2023
Time: 09:00-16:00
Venue: Chongqing International Expo Center

SEMICON Southeast Asia 2023

Date: May 23-25, 2023
Time: 10:00-17:00
Venue: Setia SPICE Arena

Highly Configurable eFlash IP Testing and Repairing Circuits Development Environment: EZ-NBIST

Date: June 8, 2023
Time: 14:00-14:30
Format: Online Live Streaming

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iSTART-TEK Develops Testing and Repair IPs with eMemory's RRAM IP

RRAM (Resistive Random-Access Memory) is a type of NVM (Non-Volatile Memory) with large storage capacity, and has the potential to replace the flash memories used in electronic products such as smart phone, AIoT (Artificial Internet of Things), IoT (Internet of Things) and automotive chips.

As the replacement of NVM, RRAM is becoming increasingly popular. Especially when the performance and energy efficiency of chips are constantly improving, RRAM has presented lower reading latency and higher writing speed. Compared to the NAND flash, RRAM also have the advantage of higher switching speed. Moreover, its power consumption is lower than NAND Flash, making it an ideal memory that can be applied in industrial, automotive, AIoT and IoT chips.

iSTART-TEK is Asia's exclusive provider of memory testing and repair solutions, offering customized EDA tools, IPs, and design services to its customers. As the automotive market heats up, major global automakers are striving to invest in R&D to produce safer, more comfortable, and convenient high-tech vehicles. iSTART-TEK has developed a testing and repair solution based on eMemory's RRAM IP, and it is expected to provide automotive developers with suitable memory self-testing solution and increase yield rates.

iSTART-TEK adopts the Behavioral Model of RRAM provided by eMemory to perform a customized IP design for memory testing and repair. This customized IP contains digital circuits for RRAM testing and repair methods. By using this customized IP, chip developers can reduce design costs and shorten the design time. In addition to the technical advantages brought by RRAM, automotive electronic chip developers can also improve chip yield rates through iSTART-TEK's customized RRAM testing and repair IPs.

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iSTART-TEK Established an Eco-system Strategic Partnership with PGC

iSTART-TEK has established an eco-system strategic partnership with Progate Group Corporation (PGC) to provide iSTART-TEK's customers with more diversified options in semiconductor foundries and packaging and testing companies.

Founded in 1991, PGC is a top 10 IC design service company in Taiwan and a certified member of TSMC Design Center Alliance (DCA). PGC focuses on ASIC design turnkey services, specializing in high-end nanometer design services for 12-inch wafer processes. It works closely with the packaging company, ASE, to provide more IP solutions to meet customers' diversified product applications and enhance their competitiveness. It has an in-house testing factory that can provide test program development services, chip probing and high/low-temperature testing services, as well as IC final testing services, offering customers integrated testing solutions in the engineering and mass production stages. Since its establishment, PGC has successfully completed over 1000 tape-out projects at TSMC for hundreds of customers, and produced over hundreds of millions of ICs.

iSTART-TEK is a leading provider of customized EDA tools and IPs, specializing in memory testing and repair solutions and customized design services. Benefiting from the ideal position in the semiconductor industry chain, iSTART-TEK has established a complete eco-system that combines IC design companies, design service companies, memory IP suppliers, wafer foundries, testing equipment suppliers, and cloud service platforms. With close integration of the eco-system, we expand the market demands and provide customers with higher added value and market competitiveness. iSTART-TEK's customized functional designs for automotive chips have made many automotive chip manufacturers choose our solutions. Today, through strategic cooperation with professional design service companies such as PGC, we can enrich our customers' options in mass production and packaging and increase their opportunities to adopt iSTART-TEK's solutions.

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iSTART-TEK and EE Solutions Join Hands to Enrich the Eco-system

iSTART-TEK and EE Solutions have joined forces to establish a strategic partnership, further enriching the eco-system members of iSTART-TEK.

EE Solutions has been continuously establishing partnerships with EDA vendors, IP/library vendors, and semiconductor foundries, adhering to the concept of "division of labor" and actively searching for new partners to face the continuous design challenges. The company's unique "hybrid" design environment uses tools from multiple EDA vendors plus internally developed tools for power, noise and die size optimization. EE Solutions has already established close cooperative partnerships with numerous solution providers, offering a rich selection of IP options and comprehensive integrated services. With strict control over customer data security, EE Solutions provides quality-oriented and standardized operational processes, coupled with flexible and customized business models, to offer customers competitive NRE pricing and assist in accelerating design and production completion. Through advanced design technologies, EE Solutions delivers optimal solutions, effective design methodologies, and a range of advanced IPs (silicon intellectual property) to assist customers in entering the field of nanometer design. Their services include specification discussions and formulation for ASIC designs, fully meeting customers' design requirements, helping resolve technical issues, and completing production development.

As Asia's only customized EDA tool and IP provider specializing in memory testing and repair in SoCs. Benefiting from its excellent position in the semiconductor industry chain, iSTART-TEK is constructing a comprehensive eco-system that integrates IC design companies, design service providers, memory IP suppliers, wafer foundries, test equipment suppliers, and cloud service platforms. Through the seamless integration of this eco-system, iSTART-TEK expands its market base, while providing customers with added values and market competitiveness.

iSTART-TEK is continuously constructing its eco-system, aiming to create a mutually beneficial community. Through a strategic partnership with EE Solutions, a professional design service company, iSTART-TEK enriches customers' options in SoC design and increases the opportunities for customers to adopt iSTART-TEK's solutions.

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Exclusively Customized Design Features for Automotive Electronics

As the global automotive industry trends towards intelligentization and electrification, the reliability test and safety features of chips for automotive electronics are becoming increasingly important to meet the AEC-Q100 specifications and enter the automotive market. iSTART-TEK's START™ v3 not only provides numerous memory testing functions and high-efficiency memory repairing solutions but also offers exclusive customized automotive electronics features, such as POT 2.0 (Power-On Test), Error-Correcting-Code (ECC) and User-Defined Algorithms (UDA). These features enable chip developers to accurately detect memory defects in automotive chips based on the applications and enhance driving safety.

I. POT 2.0 (Power_On Test)

1. Feature Introduction

POT 2.0 is an essential function for electronic products, espacially for products that are related to automotive and safety. The feature ensures memory testing of the hardware circuits after power on process, and verifies the behavioral correctness. iSTART-TEK has developed POT 2.0 with memory testing and repairing capabilities, which have been integrated into the START™ v3 tool. It allows users to incorporate memory POT functional circuits into their designs more easily, and offers the activation methods as follows.

- ROM: Storing test commands in ROM
- RTL: Storing test commands in ROM described by RTL
- Basic: Providing host_MEN signals for memory testing
- CPU: Controlling the BIST circuit by giving test instructions through the CPU

The LATCH_GO diagnostic feature can be added to the applications through marking the number of fault memory as one memory corresponding to one bit. The feature offers quick identification of memory error locations for the users. The Error Injection feature enables the insertion of error information into the Test Pattern Generator circuit to verify the correctness of the BIST circuit, significantly increasing its reliability. Additionally, when using POT 2.0, if new memory errors are detected, memory repairing can be performed.

2. Usage Methods

START™ v3 (BFL) Settings:

Set the activation methods through the "set pot" options, as shown in Figure 1.

```
set parallel_on                 = no      # yes, no
set reduce_address_simulation   = no      # yes, no
set rom_half_access             = no      # yes, no
set rom_result_shiftin          = yes      # yes, no
set rom_result_shiftout         = no      # yes, no
set specify_clock_mux           = no      # yes, no
set specify_dt_port_value       = no      # yes, no
set Q_pipeline                  = no      # yes, no
set pot                         = rom      # no, rom, hw_rom, basic , cpu
set ecc_function                = no      # yes, no
```

Figure 1 POT Setting Options

i. set pot = rom or set pot =hw_rom

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Set the pot option as "rom", and the testing commands will be stored in ROM. Set the pot option as "hw_rom", and the testing commands will be stored in the ROM described by RTL, also known as the hardwired ROM. Lastly, completing the BFL and BII workflow to generate the corresponding circuits and pins for usage.
POT consists of three main modules: ROM Memory/Hardwired ROM, ROM Controller, and MBIST/MBISR, as shown in Figure 2.

Firstly, after receiving the commands of executing the POT function, the ROM Controller will read the testing commands stored in the ROM memory/ Hardwired ROM. Next, it will send the control signals to MBIST to start memory testing. If memory errors are detected, MBISR will automatically execute the repairing workflow.

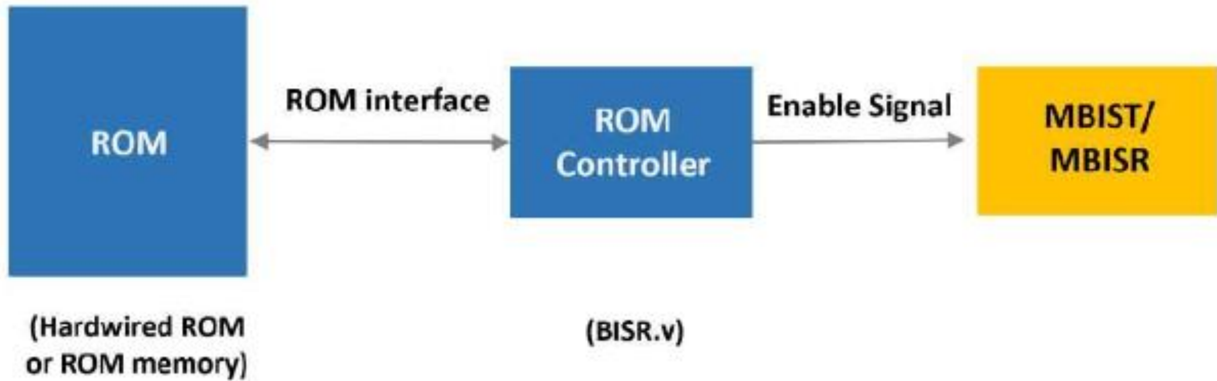

Figure 2 POT Modules

Figure 3 shows the waveforms of POT-related signals. SYS_POT is the enable signal for POT. Once the signal is activated, the ROM controller reads the test instructions from ROM memory/Hardwired ROM and initiates memory testing and repair. The test results can be obtained from the signals MGO, MRD, and RGO.

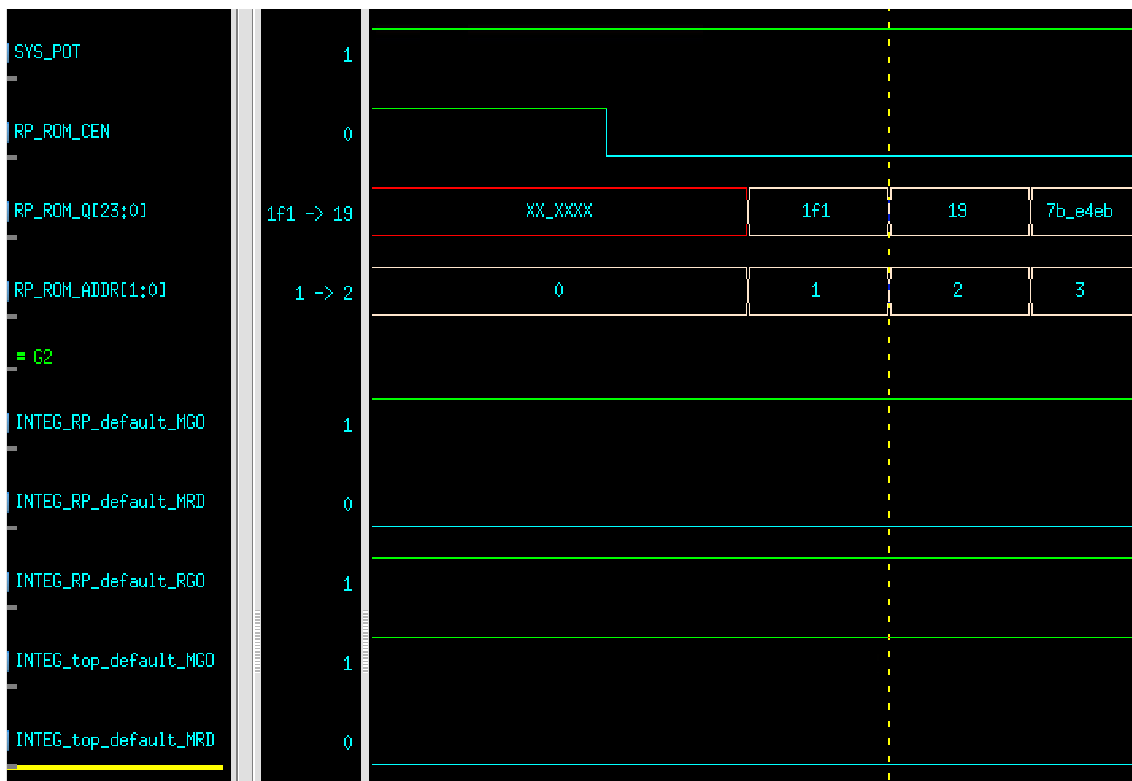

Figure 3 The Waveform of POT-related Signals

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The MBIST/MBISR signals of POT= "rom" or "hw_rom" are shown as Figure 4.

Name	Direction	Width	Description
SYS_READY	input	1	The system boot is ready to enable BISR logics (hard repair only). "1'b1": Ready to load data from NVM storage)
SYS_POT	input	1	Enable Power on test (normal function test only).
BOOT_CFG_DONE	output	1	The shifting of configuration data is completed (hard repair only). "1'b1": the scan is completed. "1'b0": the scan is progressing.
RCK	input	1	The clock signal for storage device, BISR logics and configuration buffer
RRST	input	1	The reset signal for storage device, BISR logics and configuration buffer
MRD	output	1	Indicates if the test is ended or not 0: The test is uncompleted. 1: The test is ended.
MGO	output	1	Indicates if the test is failed or not 0: The test is failed. 1: The test is passed.
RGO	output	1	Indicates if the logic can be repaired or not 0: The logic cannot be repaired. 1: The logic can be repaired. (MBISR CTR only.)

Figure 4 The MBIST/MBISR Signals of rom and hw_rom

Finally, the Verilog file containing the test commands to be stored in ROM will be generated. It will generate the corresponding commands based on the BIST functions designed by users, as shown in Figure 5. The Verilog program example in Figure 6 shows the test commands stored in the ROM described by RTL.

```
@00000000 000000039 // digital_top_with_pad_digital_top_default ['TRANS : 0',
'PRL_ON : 1', 'GRP_EN : 11', 'MEB_ID : 00', 'MEN : 1']
@00000001 000359b6c // GOLD_SIGNATURE_1 {'ctr_name':
'digital_top_with_pad_digital_top_default', 'rom_tpg_position':
'digital_top_with_pad_digital_top_default_tpg_2_1_1'}
@00000002 0009442a9 // GOLD_SIGNATURE_2 {'ctr_name':
'digital_top_with_pad_digital_top_default', 'rom_tpg_position':
'digital_top_with_pad_digital_top_default_tpg_2_1_2'}
@00000003 000b204e4 // GOLD_SIGNATURE_3 {'ctr_name':
'digital_top_with_pad_digital_top_default', 'rom_tpg_position':
'digital_top_with_pad_digital_top_default_tpg_2_1_3'}
```

Figure 5 The Test Commands Stored in ROM

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```
module rom_24_hw (
CLK,
A,
CEN,
Q
);
```

```
input           CLK;
input [2:0]     A;
input           CEN;
output [23:0]   Q;
reg [23:0] Q;

always@(posedge CLK)
 begin
  if(~CEN) begin
   case(A)
    0 : begin
        Q <= 24'h000039; // digital_top_with_pad_digital_top_default ['TRANS : 0',
'PRL_ON : 1', 'GRP_EN : 11', 'MEB_ID : 00', 'MEN : 1']
    end
    1 : begin
        Q <= 24'h359b6c; // GOLD_SIGNATURE_1 {'ctr_name':
'digital_top_with_pad_digital_top_default', 'rom_tpg_position':
'digital_top_with_pad_digital_top_default_tpg_2_1_1'}
    end
    2 : begin
        Q <= 24'h9442a9; // GOLD_SIGNATURE_2 {'ctr_name':
'digital_top_with_pad_digital_top_default', 'rom_tpg_position':
'digital_top_with_pad_digital_top_default_tpg_2_1_2'}
    end
    3 : begin
        Q <= 24'hb204e4; // GOLD_SIGNATURE_3 {'ctr_name':
'digital_top_with_pad_digital_top_default', 'rom_tpg_position':
'digital_top_with_pad_digital_top_default_tpg_2_1_3'}
    end
   default : Q <= Q;
  endcase
 end
end

endmodule
```

Figure 6 The Verilog Code of the Hardwired ROM

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ii. set pot = basic

When the POT option is "basic", the host_MEN signal line is generated for users to activate memory testing. The results can be obtained through the MGO, MRD and RGO signals. The signal list generated by the "basic" option is shown in Figure 7.

Signal Name	Description
*_host_MEN:	Indicates to enable or disable MBIST/MBISR.
*_MRD	Indicates if the test is ended or not. 0: The test is uncompleted 1: The test is ended
*_MGO	Indicates if the test is failed or not. 0: The test is failed 1: The test is passed
*_RGO	Indicates if the logic can be repaired or not. 0: The logic cannot be repaired. 1: The logic can be repaired. (MBISR CTR only.)

Figure 7 The MBIST/MBISR Signals of the "basic" Option

iii. set pot = cpu

By setting the POT option to "cpu", users can directly control the BIST circuit, and the settings can be adjusted through the .bfl file for additional features, as shown in Figure 8. For example, the LATCH_GO signals can be added to the diagnosis_memory_info function, allowing users to identify the memory number of occurring errors quickly. Figure 9 shows an example that an error occurs in memory number 6.

```
set diagnosis_support          = no     # yes, no
set diagnosis_data_sharing     = no     # yes, no
set diagnosis_memory_info      = no     # yes, no
set diagnosis_time_info        = no     # yes, no
```

Figure 8 The Latch_GO Setting on BFL

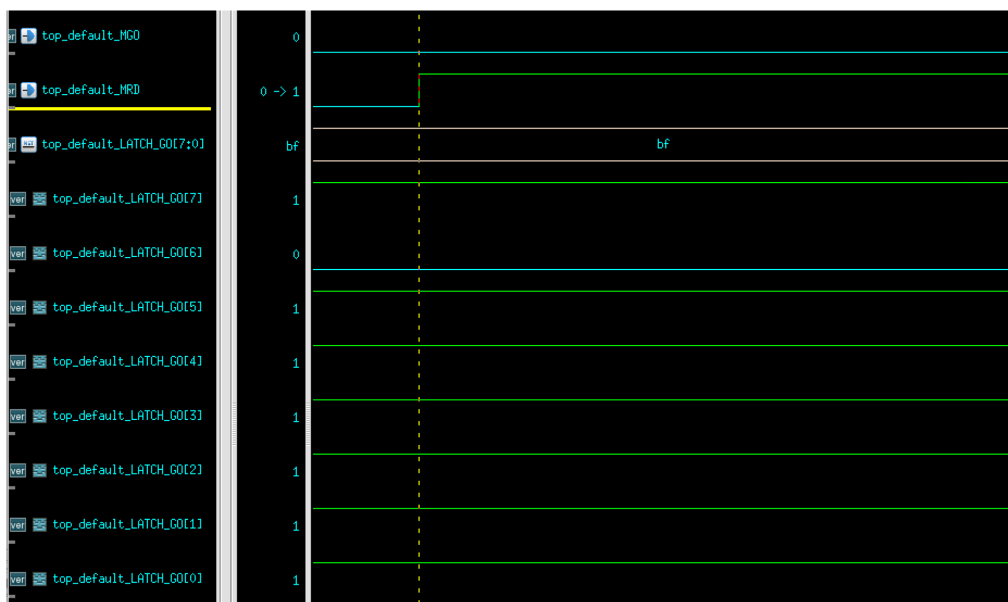

Figure 9 LATCH_GO Waveform

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II. Error-Correcting-Code (ECC)

1. Feature Introduction

Error-Correcting-Code (ECC) is an encoding method that allows the detection and correction of errors while transmitting. It can be applied to various data transmission and storage operations, where the receiving end uses the encoded data to detect and correct transmission errors. On applying to the memory, ECC can check the correctness of data stored in memory through its circuits.

Memory failures cause serious consequences on various fields including automotive, industry, medical industry, and communication. The functionality of ECC improves the stability and reliability of chips during operation.

iSTART-TEK provides ECC functionality that enables users to detect 2 bits errors and correct 1 bit error. When featuring ECC, the memory needs to allocate space for parity check to reconstruct the corrected data. The required space can be calculated as $2^{\text{Parity-1}}$ > Parity + Data bit. For example, if the memory data length is 22 bits, 6 bits of ECC space must be saved to check 16 bits of data.

2. Usage Methods

START™ v3 (BFL) Setting:

Adjust the options of set ecc_function to add ECC function and set the ECC name using the "set ecc_prefix" command, which are shown in Figure 10.

```
set ecc_prefix              = top_ECC

set Q_pipeline                  = no
set repair_mode                 = yes
set soft_repair                 = yes
set ecc_function                = yes          #ecc function
set skip_bist_path              =
```

Figure 10 ECC Setting Options

After executing the BFL and BII workflow, it generates the encoder and decoder circuits of the ECC function, shown in Figure 11 & 12.

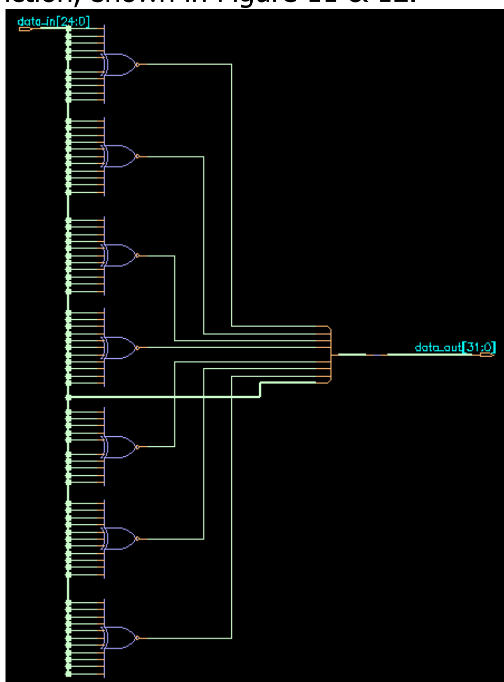

Figure 11 Encoder Circuit

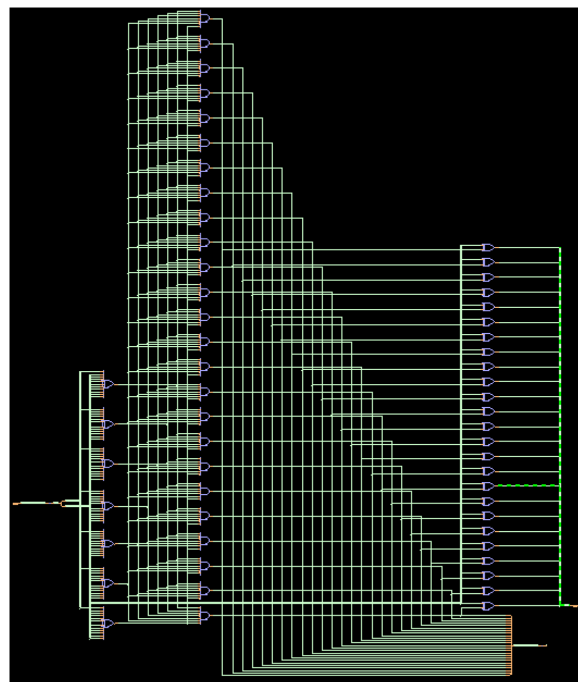

Figure 12 Decoder Circuit

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Figure 13 shows the ECC waveforms, and the data_noise signal represents the data in the memory along with the encoded checking value. By decoding it, the correct data can be obtained, also allowing data correction.

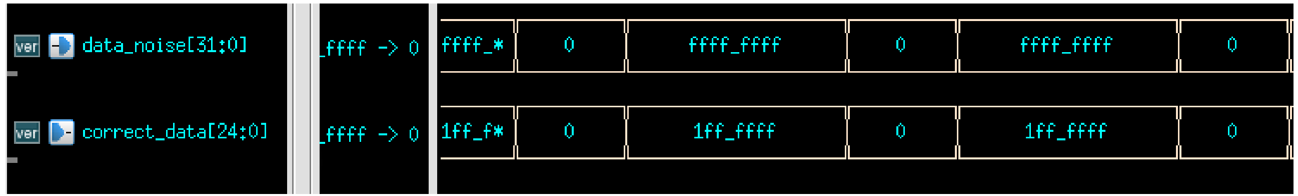

Figure 13 The ECC Waveform

II. UDA (User Defined Algorithm)

1. Feature Introduction

As technology evolves, newly developed advanced process memories combine with commonly used algorithms can result in longer testing time and behaviors of repeating testing patterns. For example, if users select both the March C^+ (14N) and March C^- (11N) algorithms, the testing time will be 25N.

March C+	>(wa) >(ra,wb,rb) >(rb,wa,ra) <(ra,wb,rb) <(rb,wa,ra) <(ra)
March C-	>(wa) >(ra,wb) >(rb,wa) >(ra) <(ra,wb) <(rb,wa) <(ra)

iSTART-TEK has developed the User Defined Algorithm (UDA) feature, which allows users to customize and edit algorithms. With this feature, repetitive elements can be removed, resulting in a shortened testing time of 23N.

>(wa) >(ra,wb,rb) >(rb,wa,ra) <(ra,wb,rb) <(rb,wa,ra)
>(ra,wb) >(rb,wa) >(ra) <(ra,wb) <(rb,wa) <(ra)

UDA is represented in the form of components, which can be regrouped and combined to generate new algorithms as shown in Figure 14.

Syntaxes	Functions
UP	Address counted up from 0
DN	Address counted down from the maximum value
ADD_INC	Address+1 or Address-1 decided by UP or DN
N	No operation
R(A)	A is marked as the processed pattern for the Read operation
W(A)	A is marked as the processed pattern for the Write operation
S	The memory testing has entered the sleeping state, and the sleeping time is defined by users.
,	Segment different operations
;	Complete the present elements

Figure 14 UDA is Represented in the Form of Components

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UDA provides a friendly graphical user interface (GUI) that enables users to startup quickly, which is shown in Figure 15.

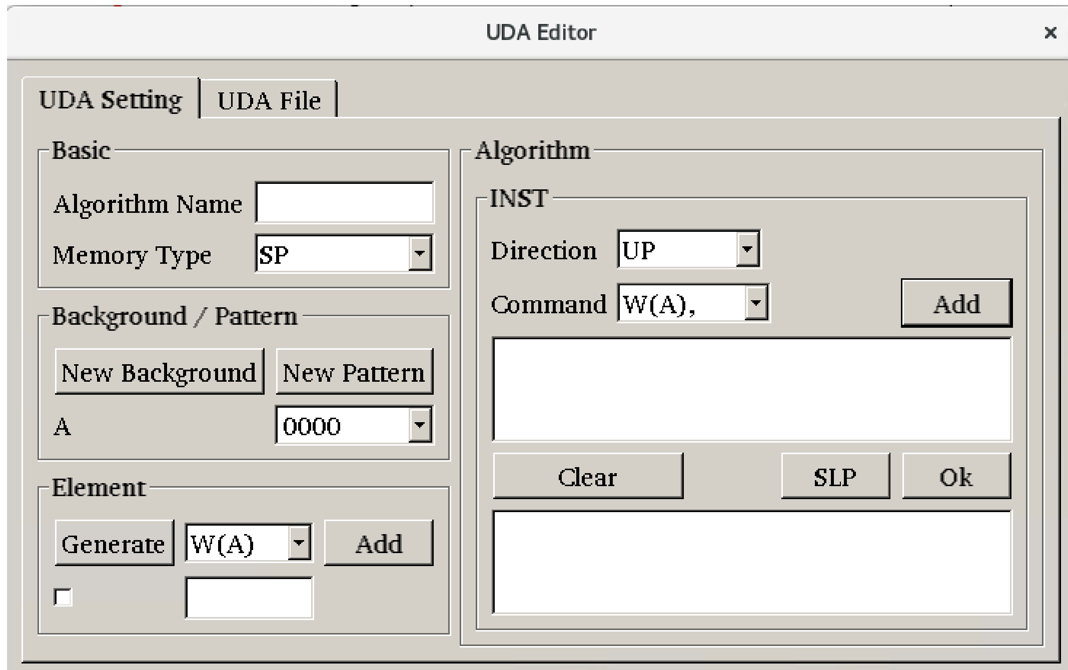

Figure 15 Graphical User Interface of UDA

2. Usage Methods

Through the GUI of UDA, users can quickly set the components. An overview of the blocks in the GUI is displayed in Figure 16, enabling easy setup of test patterns, read/write operations, and address increments/decrements. Once completed, the corresponding algorithm is generated.

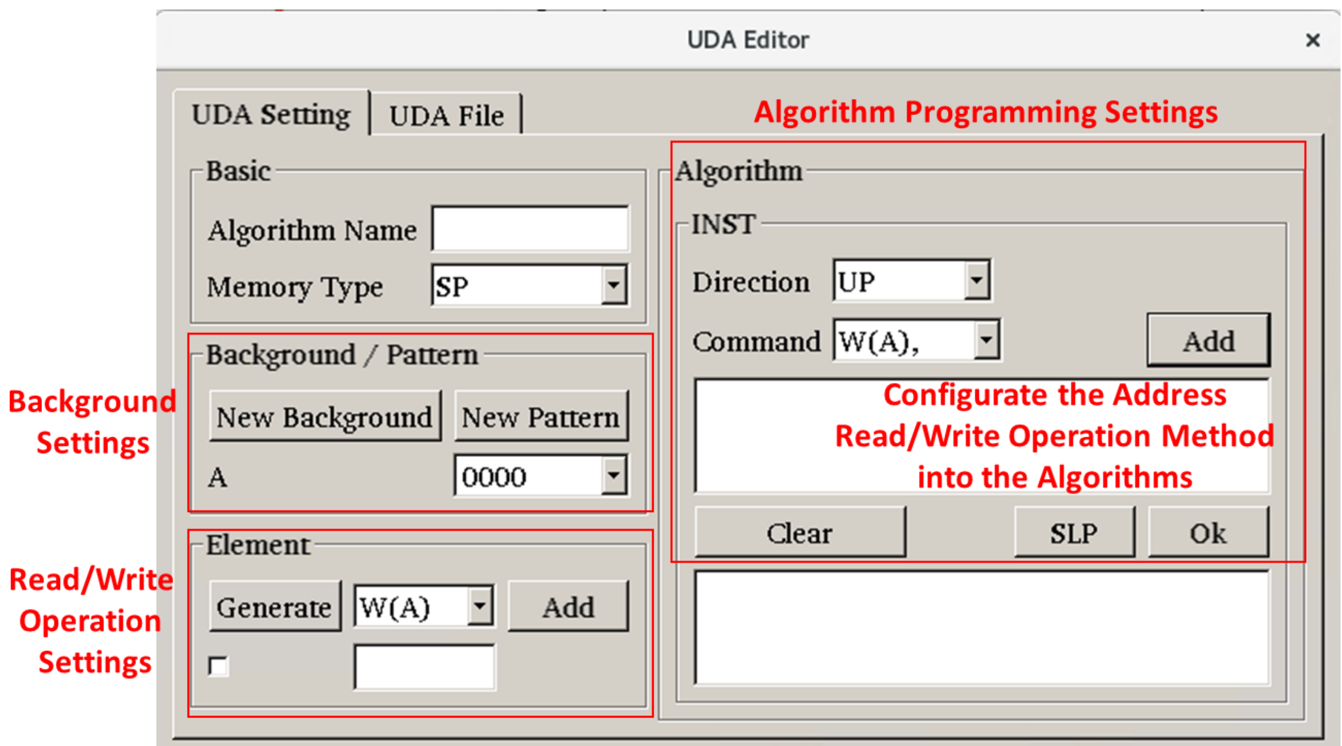

Figure 16 Overview of GUI

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Taking a March C algorithm as an example: After completing the algorithm settings with the GUI, click the UDA file, and the algorithm setting results will be displayed. Then click "Export" to export the algorithm as a .txt file. Lastly, in the .bfl configuration file, specify the paths of the aforementioned .txt files. Once completed, the BIST circuits corresponding to the algorithm are generated as shown in Figures 17, 18, and 19.

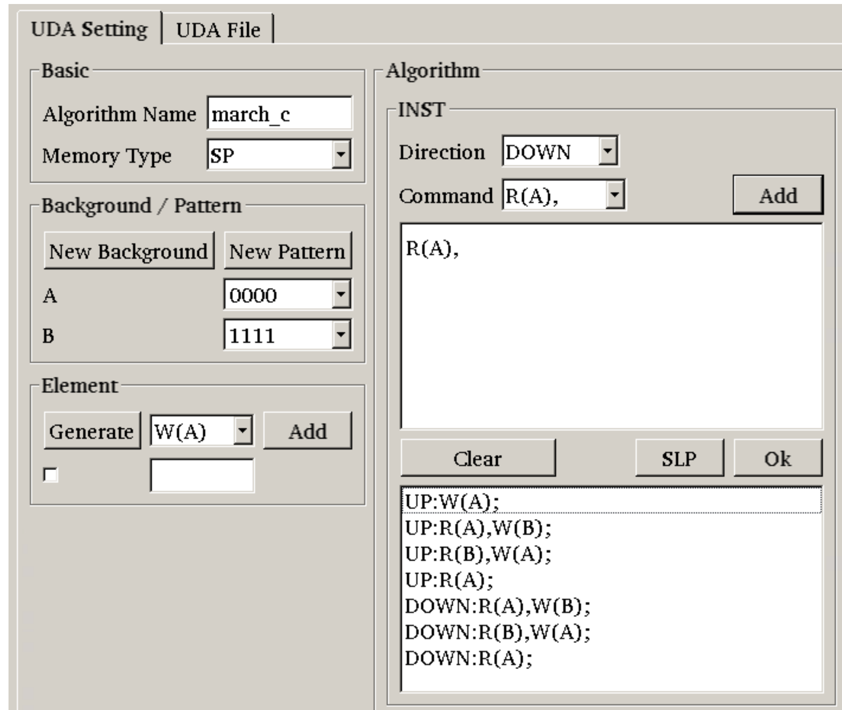

Figure 17 Configuration of March C Algorithm

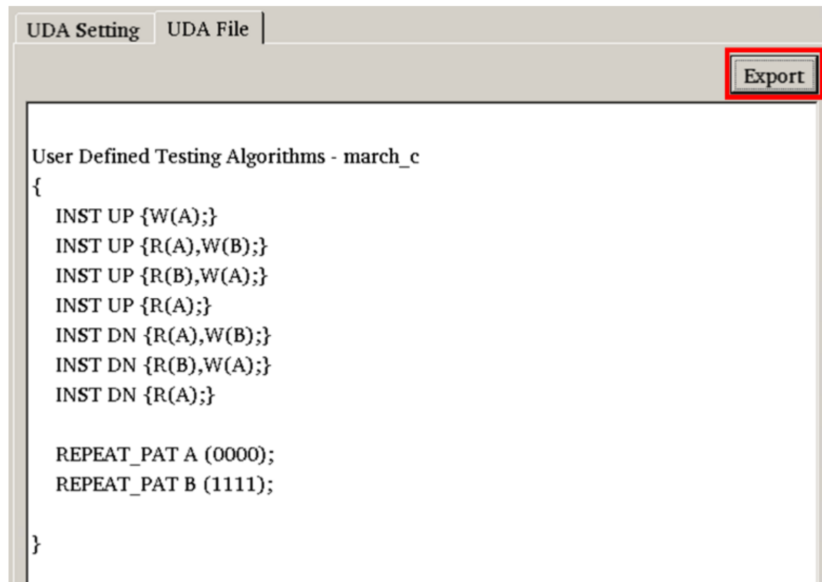

Figure 18 Export the Algorithm

```
define{user_define_algorithm}
  set SP_alg_path = ./UDA/uda_march_5w.txt
end_define{user_define_algorithm}
```

Figure 19 Configuration of a UDA File

Authored by iSTART-TEK

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Highly Configurable eFlash IP Testing and Repairing Circuits Development Environment: EZ-NBIST

1. Testing methodologies of NVM IP

The testing methodologies of eFlash IP covers full wafer sort, and final test for UMC's 40nm, 55nm and SST's 0.11um, 0.18um and customized embedded eFlash IP.

iSTART-TEK develops EZ-NBIST GUI tool to save BIST coding time of NVM IP.

EZ-NBIST follows eFlash vendor's testing methodologies to implement all test items' timing diagrams and save parallel long testing time in ATE.

2. Why NVM IP needs to use BIST and BISR?

NVM IP has complicated testing functions to cover each disturbing condition. The memory BIST adds logic to an IC which allows the SoC to test its own memory operation.

MBIST tests the eFlash macro through an effective test algorithm to detect possibly all the faults. MBIST generates test patterns from eFlash vendor requirement to the eFlash macro and reads them to find any eFlash defects.

BISR adds repair circuit to backup memory to increase the eFlash IC yield.

3. How iSTART-TEK accomplish BIST and BISR of NVM IP?

iSTART-TEK develops EZ-NBIST GUI tool to generate BIST and BISR of eflash IP.

iSTART-TEK BIST implements all eFlash test items to cover wafer soft and final test. BIST interface is a flexible serial interface to reduce IC test pins. Increase BIST test flexibility, all test items can be enabled and disabled individually. Provide diagnosis mode to debug defect address.

iSTART-TEK BISR records eFlash faulty memory address and use redundancy sectors to increase eFlash IC yield. Provide auto repair function.

Figure 1 shows eFlash test and repair solutions.

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- Timing parameters can be adjusted
- Provide repair mode to increase yield
- Implement all recommendation test items for high test coverage
- Provide diagnosis mode
- All test item can be enabled and disable
- Interface
  - JTAG, IEEE 1149.7, SPI
- Security code protection

Figure 1

Figure 2 shows eFlash test and repair features.

- System testing max clock: 16MHZ Up
- JTAG clock: 10MHz~50MHz
- Read BIST result to get pass/fail
- Support configurable to 16Kx128 (UMC) , 64Kx144 (UMC), 128Kx32 (SST), and 16Kx32 (SST) size
- Support generating ATE STIL/WGL format
- Provide diagnosis information

Figure 2

Figure 3 shows eFalsh diagnosis simulation output.

```
item cnt: 374
addr:     1
fault_bit:00000000000000000000001000000000000

item cnt: 374
addr:   255
fault_bit:00000000000000000000001000000000000

item cnt: 374
addr:   511
fault_bit:00000000000000000000001000000000000

item cnt: 374
addr:   521
fault_bit:00000000000000000000001000000000000

item cnt: 374
addr:   541
fault_bit:00000000000000000000001000000000000
```

Figure 3

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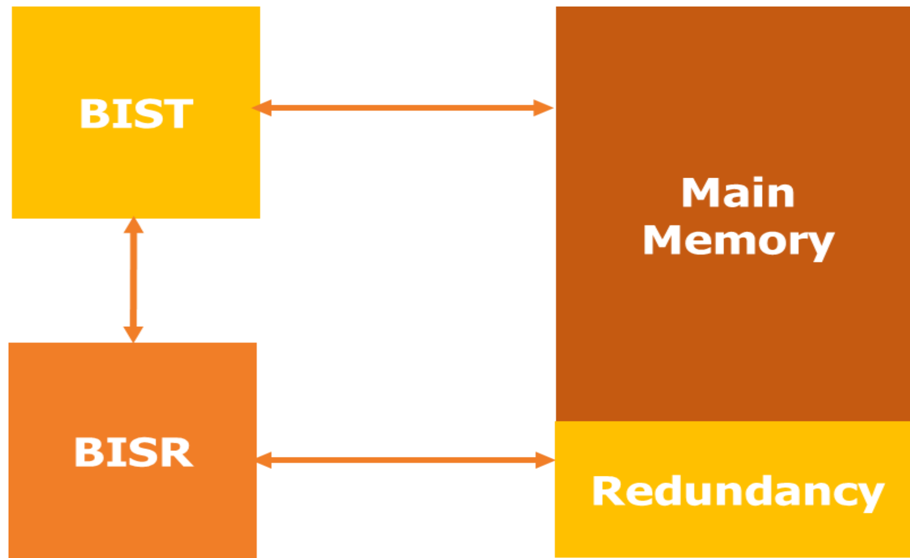

Figure 4

4. What is EZ-NBIST?

EZ-NBIST is an NVM GUI tool to generate BIST and BISR of NVM IP.

Figure 5 shows the perspective of EZ-NBIST GUI. Click "EZ-NBIST Config" from "Config" drop-down menu.

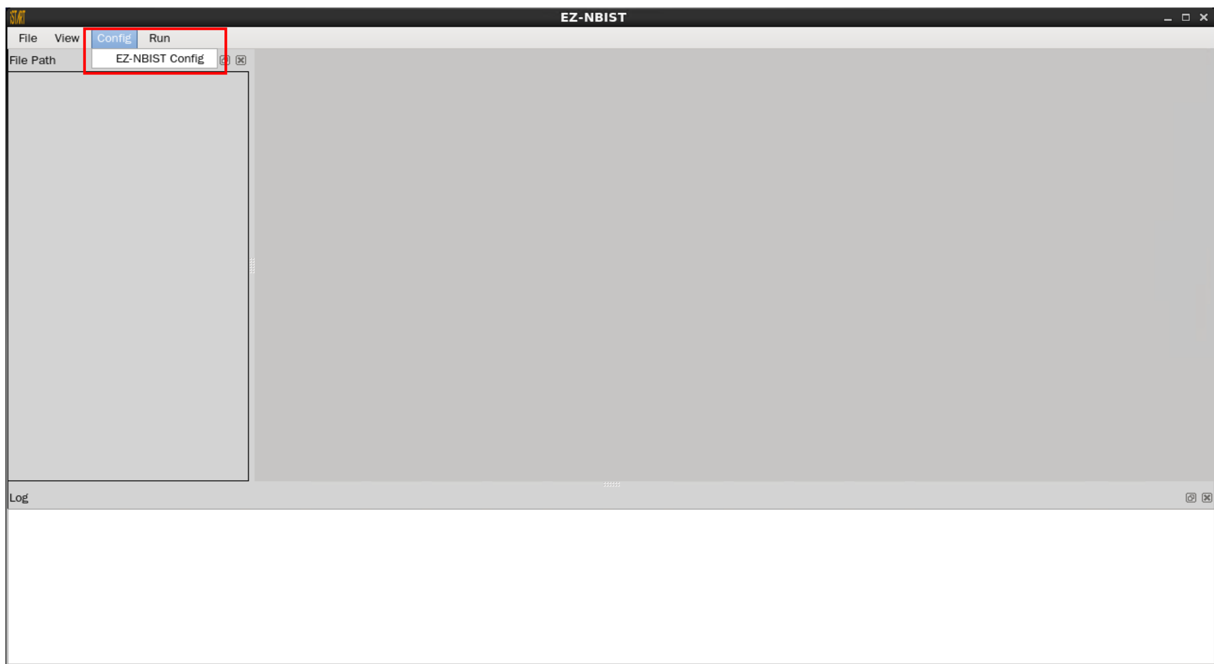

Figure 5

Users click "Run..." from "Run" drop-down menu to execute EZ-NBIST.

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Figure 6

5. How many NVM IP are included in EZ-NBIST?

EZ-NBIST GUI supports following eFlash IP for UMC 64Kx144, UMC 16X128, SST 128Kx32, SST 16Kx32 IP sizes and customized IP sizes.

Users can choose UMC, SST and customized eFlash macro types, vendor types and specific eFlash macro sizes as shown in Figure and Figure .

Figure 7

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Figure 8

6. What kinds of interface are included in EZ-NBIST?

EZ-NBIST GUI supports 3 flexible serial interfaces JTAG, IEEE1149.7, and SPI as shown in Figure 9.

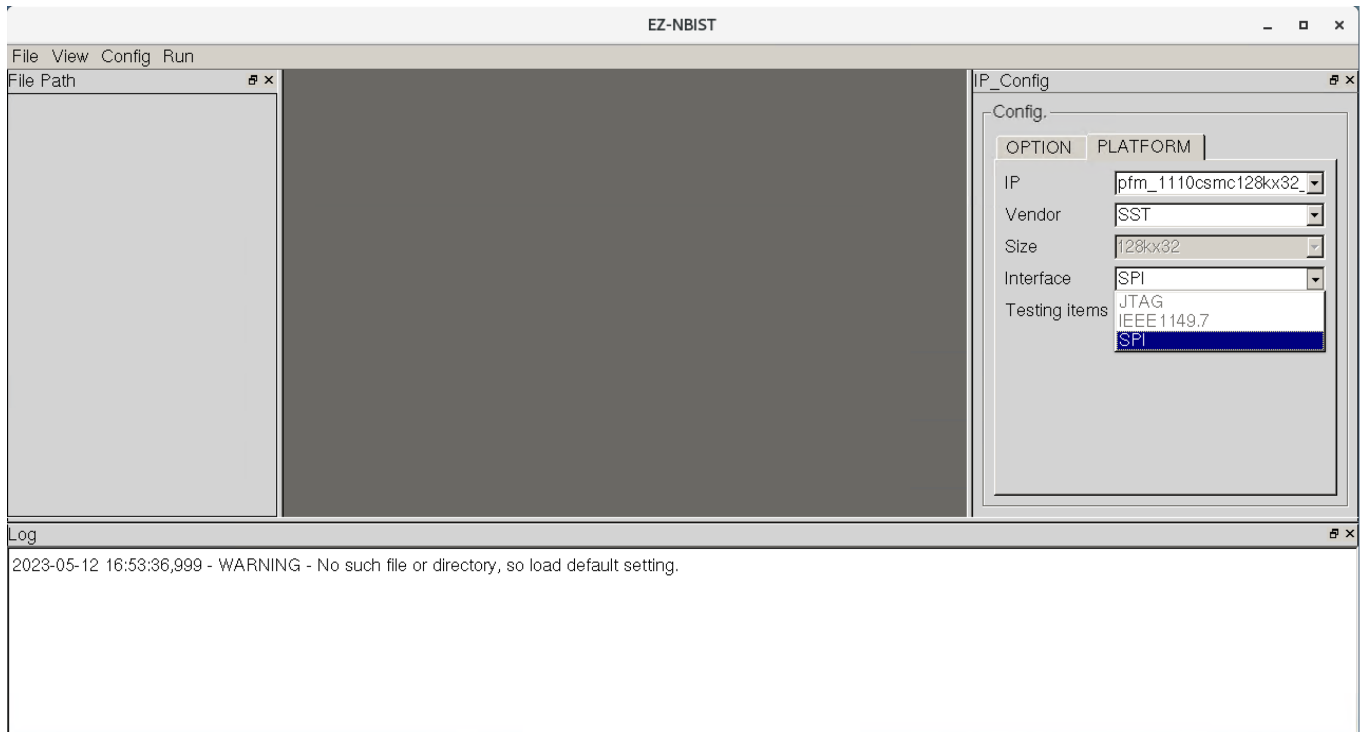

Figure 9

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Figure 10 shows eFlash test and repair block with JTAG interface.

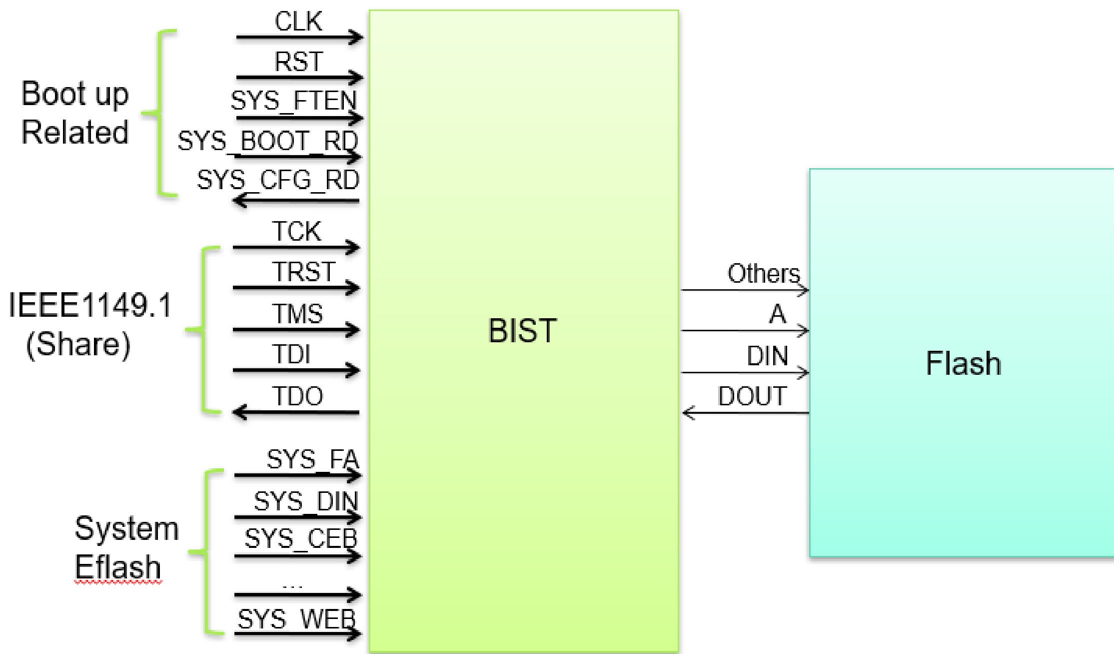

Figure 10

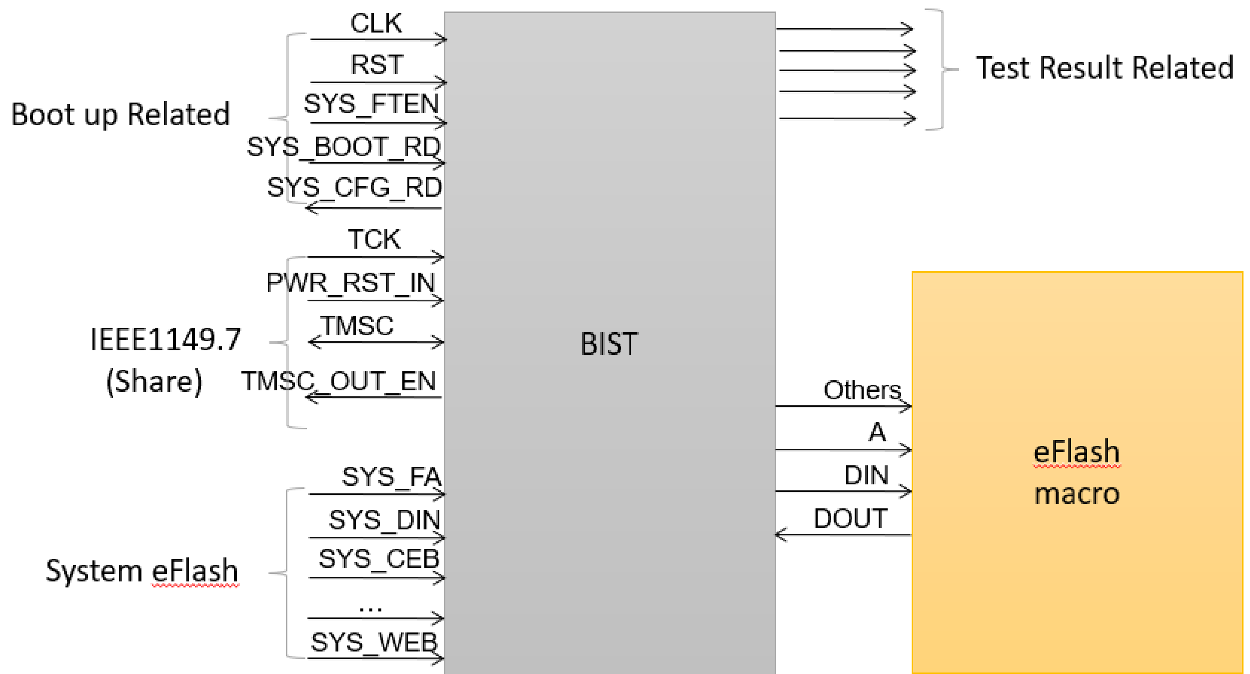

Figure 11

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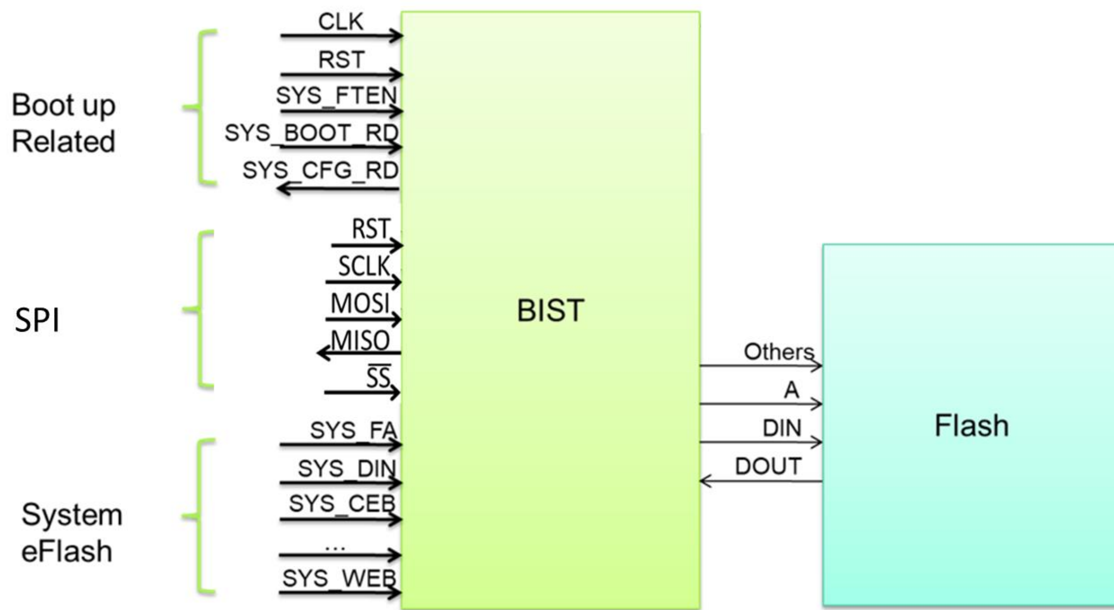

Figure 12

7. How flexibility of EZ-NBIST?

EZ-NBIST supports configurable BIST and BISR IP for different eFlash macro sizes. All eFlash timing parameters can be adjusted. Figure 13 shows all test items can be enabled and disabled individually.

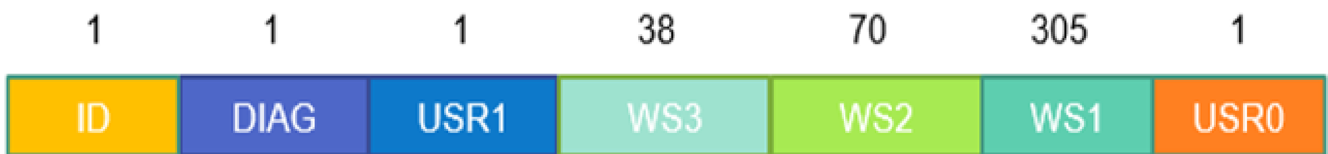

Figure 13

EZ-NBIST can help users to generate the complete synthesis RTL, the verification environment, the testing patterns, the behavior model, and the customized eFlash database as shown in Figure 14.

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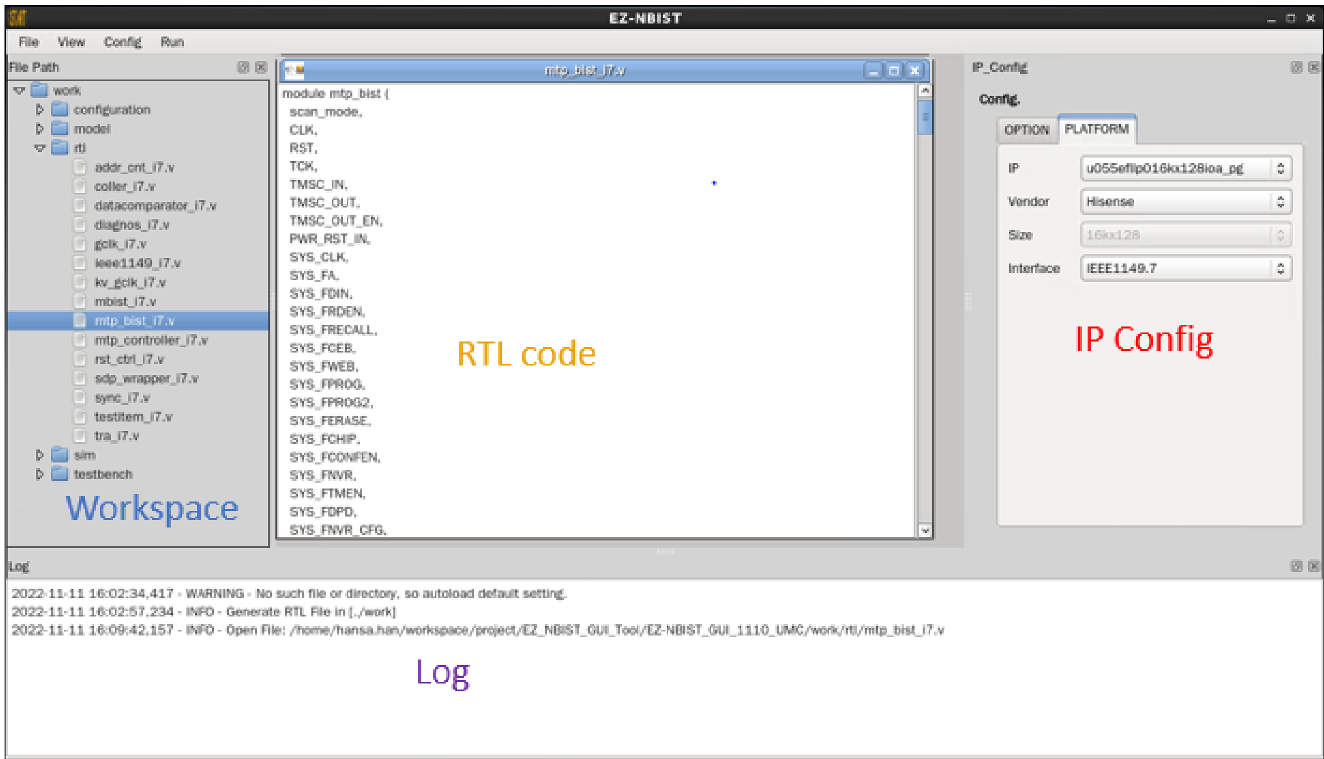

Figure 14

To execute simulation with eFlash model, users can select a test pattern to generate simulation dump files. For example, execute "2" in Figure 15 to start "ws1" testing item's simulation flow.

```
1  1149        check dr1=10..01, dr2=2, dr3=3, dr4, ten= 1,0,1,1,0,0,1
               check tdo=10'b10_0000_0001 when ir=5
               check tdo=32'hffff_ffff when ir=6
               check clear_ten and ten
2  ws1         check ws1 test item
3  ws2         check ws2 test item
4  ws3         check ws3 test item
5  ws1_trim    check ws1 trim function
6  ws1_repair  check ws1 repair function
7  repair      check ws2 test item, has_fault
8  repair_fail check ws2 test item, has_fault
9  diagnosis   check ws2 test item, has_fault
10 normal_test check normal function
```

Figure 15

8.Conclusion

EZ-NBIST provides UMC and SST eFlash BIST/BISR with professional testing items. EZ-NBIST saves eFlash tuning parameter timing time in ATE. The eFlash BIST and BISR area overhead of SoC is acceptable. EZ-NBIST is also easy to set for accomplishing eFlash IP's testing circuit.

Authored by Hansa Han, iSTART-TEK

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iSTART-TEK is Invited to Participate in the CAD Contest Proposition

As the chip complexity and design difficulty increase, IC design requires the assistance of electronic design automation (EDA) tools to create low-power, high-performance, and cost-effective products. In light of this, the Ministry of Education has organized the CAD-related contests and events to promote the development of EDA tools. iSTART-TEK, an EDA tool and IP provider that specializes in memory testing and repair, has participated in the proposition of this year's "CAD Contest" held by the Ministry of Education.

Currently, CAD contest is one of the most important international contests in the EDA field. The design concept for this contest focuses on "developing lossless data compression algorithms and lossless data restoration." Through algorithm design and program implementation, the optimization of memory repair data compression can be achieved. Participants were supposed to complete compression and decompression executables while minimizing the compression rate and execution time within a limited time frame. The contest not only tested participants' expertise and programming skills but also their attentiveness and perseverance. iSTART-TEK expected to strengthen our presence in the academic community and fully leverage the benefits of collaboration among industry, academia, and government.

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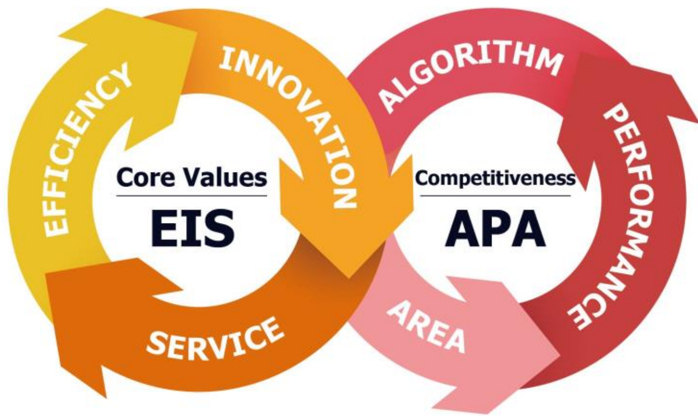
MR Semi, iSTART-TEK's Valued Customer, Wins the "Best MCU of the Year" Award

Congratulations to MR Semiconductor Ltd. (MR Semi), a valued customer of iSTART-TEK, for winning the "Best MCU of the Year" award at the 2023 China IC Design Awards! Their flagship MCU, MR88F001, was recognized as the top MCU product in the industry.

Enhance Chip Competitiveness for IC Design Companies with iSTART-TEK's Products



ARM, a major IP (intellectual property) provider, is reported to be planning to change its business model in 2024. Instead of the previous charging method based on chip prices, it will adjust to charging a certain percentage based on the average selling price of terminal products. The new business model is expected to affect the average cost of chips.

Based on iSTART-TEK's core values of (Efficiency, Innovation and Service), we provide products with optimized APA (Algorithm, Performance and Area), which are supposed to help IC design companies reduce chip development costs and increase competitiveness.

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UnicomSemi, iSTART-TEK's Customer, Achieves Milestone in Supporting ISO 15118 Plug & Charge

UnicomSemi, a smart charging communication chip design company, offers a solution supporting ISO 15118 Plug & Charge for simplified electric vehicle charging. This feature simplifies the charging process, as the charging station automatically identifies the vehicle information, eliminating the need for manual verification by users before charging.

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