iSTART iReport

iSTART TEK INC.

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iSTART-TEK's Quality Management:

ISO 9001:2015 Certified

iSTART-TEK, Asia's only EDA tool and IP provider of memory testing and repair solutions, is excited to announce that we have successfully obtained ISO 9001:2015 Quality Management System certificate.

Quality control is the critical factor in the success of many outstanding enterprises, as it helps to ensure them to provide customers with satisfactory products and services. Since its establishment, iSTART-TEK has been dedicated to providing memory testing and repair solutions, as well as customized design services with attention to every detail. By closely collaborating with customers, we help them build optimized memory testing and repair methods. We are committed to optimizing and standardizing our management systems to improve the effectiveness of our operations, elevate our management standards, and drive the rapid growth of our company.

Stated by iSTART-TEK, this ISO 9001 certification audit is a comprehensive inspection of the company's operations. Obtaining the ISO 9001:2015 Quality Management System certification indicates that iSTART-TEK's quality management system as well as memory testing and repair solutions meet the ISO standard, and is able to provide customers with stable and high-quality services. We will never stop progressing and improving our service quality, ensuring our international competitiveness.

POT 2.0 Wins Favor of More Automotive Chip Suppliers

iSTART-TEK is Asia's only company that specializes in memory testing and repair solutions, providing customized design services, EDA tools and IPs. As the automotive market heats up, global automakers are focusing on how to produce safer, more comfortable and convenient high-tech vehicles.

iSTART-TEK's loyalty contracts are mainly from automotive chip suppliers. The reason that STARTTM v3 and EZ-BIST have gained the favor of automotive electronic chip suppliers in the past is that their exclusive POT 1.0 function for automotive chip design fully met the design requirements of automotive chip developers.

Recently, iSTART-TEK has introduced the exclusive "POT (Power_On Test) 2.0" function in STARTTM v3 and EZ-BIST for automotive chips. POT 2.0 not only helps developers to develop electronic components that are more cost-effective, better quality, and meet regulations, but its simple and user-friendly features also greatly satisfy many developers.

POT 2.0 can be utilized in more cases, including recording the test process in ROM (Read-Only Memory) to control use cases, controlling use cases in the form of RTL or with a signal, and even controlling use cases through the CPU (Central Processing Unit).

POT 2.0 also includes a new feature, "Real-Time Memory Monitoring" after power-on. This allows for immediate memory testing and repair of any errors found in the chip after power-on. The " Real-Time Memory Monitoring" feature also conducts testing on the repaired memory to ensure it is functioning properly and maintaining normal operation. Another new feature in POT 2.0 is "Error Injection", which is to ensure the accuracy of the memory test circuit, and supports iSTART-TEK's patented "accumulated memory test and repair solution". This allows for immediate memory testing and repair after power-on. When there are enough backup memories, it can proceed with repeated testing and repair of the chip's memory along with the "Real-Time Memory Monitoring" feature, ensuring that the automotive electronic chip meets all safety regulations.

iSTART-TEK stated that the features of POT 2.0 have strengthened the safety design of STARTTM v3 and EZ-BIST for automotive chips. It also enables iSTART-TEK to win more contracts from automotive chip suppliers.

The Diagnosis Tool for Memory Testing and Development of Automotive SoCs

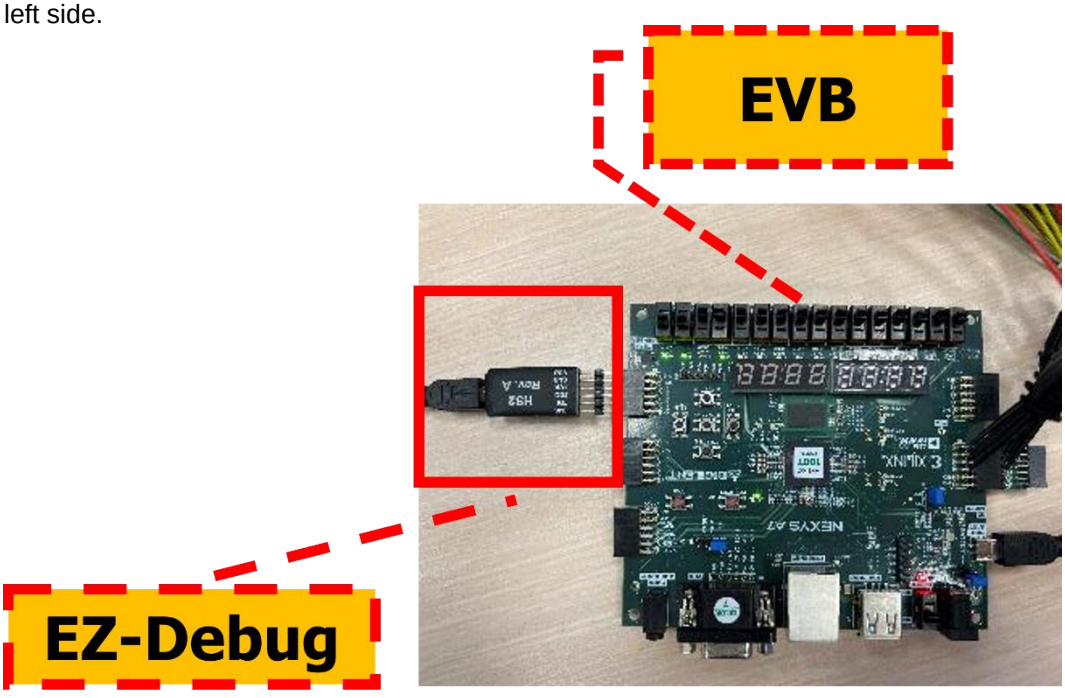
Automatic test equipment (ATE) is commonly used for SoC testing. The ATE then generates a log file of the testing results. When the ATE log file is only consist of the signals 0 or 1, this log file is not easy to understand without using analysis tool. To simplify and expedite the analysis of ATE testing results for memories, the ATE diagnosis tool of START™ v3 is introduced. Along with the files generated by iSTART tools, it can easily analyze faulty memory information. iSTART has also developed a PC-based JTAG-to-USB debugging tool EZ-Debug that can debug some chips after shuttle tape out or chips under development. This tool helps reduce ATE testing costs and obtain real-time diagnosis results.

I. EZ-Debug (JTAG-to-USB Debugging Tool)

1. The block diagram of the EZ-Debug

   The EZ-Debug debugging tool makes diagnosis convenient by allowing communication between the PC and FPGA through an adapter cable. This tool is primarily used for simulating some chips after shuttle tape out or chips under development. The adapter cable and tool specifications are shown in the figure below. The PC connects to the adapter cable via USB, and the adapter cable and tool convert the signals to JTAG (IEEE 1149.1) for FPGA/IC diagnosis.

The figure below shows actual usage. The red box indicates the adapter cable, with the FPGA on the right side and the PC on the left side.



2. Actual Applications:
   Start by referring to the "bist_testing" task in the complete INTEG testbench. In this task, we can find information about "CMD_DATA" as shown in the figure below. Then, fill in the input binary value based on the information in the figure and use TDI of JTAG (ieee1149.1) to do send_command to start testing.

```
top_default_CMD_DATA = {top_default_DIAG, top_default_ALG,
                        top_default_SEQ_ID, top_default_GRP_ID,
                        top_default_MEB_ID, top_default_MEN};
```

   Signal Interpretation:
   Controller_name_DIAG: It determines whether to execute the diagnosis or not. When set to 1, it will be activated.
   Controller_name_ALG: When the program_algorithm in the BFL option is enabled, the Controller_name_ALG command will be generated in the testbench to control the algorithm that is to be tested.
   Controller_name_SEQ_ID, Controller_name_GRP_ID and Controller_name_MEB_ID: These are used to specify the memory IDs that are to be tested.
   Controller_name_MEN: It is the command to enable the Controller BIST. When set to 1, it will be activated.

The TDO of JTAG will generate capture_commad. Users can interpret the content of capture_commad by referring to the “test_result” signal arrangement in the INTEG testbench shown in the figure below.

```
{top_default_MGO, top_default_MRD,
top_default_SRD, top_default_LATCH_GO} = top_default_test_result;
```

   Signal Interpretation:
   Controller_name_MGO: This is the BIST testing result. It will be 0 when the BIST testing fails.
   Controller_name_MRD: It will be 1 when the BIST testing is completed.
   Controller_name_SRD: It will be 1 when diagnosis data is ready and can be captured.
   Controller_name_LATCH_GO: The width of this signal depends on the memory amount in the meminfo file generated by START™. When each signal in LATCH_GO changes from 1 to 0, it means that the memory testing fails.

II. ATE Diagnosis Tool

START™ v3 (BFL & BII) Settings:

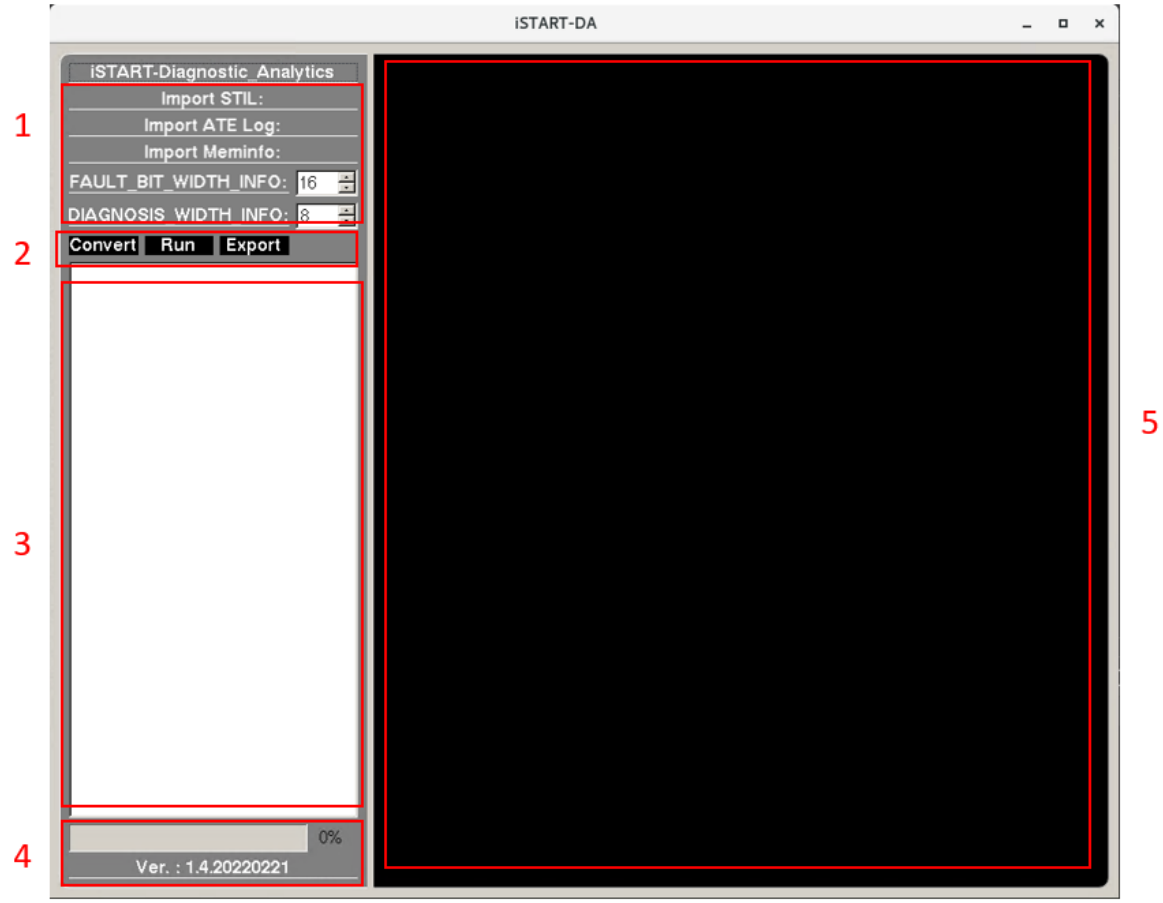
1. *.bfl Settings
   - A. diagnosis_support and diagnosis_width_info Settings
     - i. diagnosis_support: START™ v3 provides a diagnosis mode and reports diagnostic information.
     - ii. diagnosis_width_info: Align the length of test information to facilitate diagnosis and interpretation.
   - B. diagnosis_faulty_items: This provides users with the option to select diagnostic information for their own designs, including algorithms, algorithmic units, algorithmic elements, memory grouping locations, memory addresses, and memory data.

```
define{BIST}
      set diagnosis_support          = yes        # yes, no
      set diagnosis_width_info       = yes        # yes, no
      set diagnosis_faulty_items     = algorithm, operation, element, seq_id, grp_id, address, ram_data, rom_data
```

2. *.bii Settings :
   - A. Under define{Testbench}[INTEG_tb], choose the STIL as file_format to generate a memory test pattern STIL file after simulation.

```
define{Testbench}[INTEG_tb]
    set pll_wait_cycle      = 10
    set reset_cycle         = 10                # integer bigger than 0
    set file_format         = STIL            # verilog, STIL
```

Introduction of the Diagnosis Tool Interface:



1. Files and Settings:
   A. Import the STIL file for ATE: The STIL file will generate the corresponding memory test pattern based on the options set in START™ v3 (as the START™ v3 settings mentioned above).
   B. ATE log: It is the file of the ATE testing result.
   C. meminfo File: This is generated by START™ and it contains all the information of the memories.

```
# if the instance is the alais type , The ** is .
[DOMAIN=top_default, cycle=100.0ns]
     [CTR] # Hier: top
         [SEQ] # No.= 1,InstanceNo= 3,SEQ_max_addr_size= 1024,Hier: top u_t1
             [GROUP] # No.=1_1
                   [SP=1_1_1, byp=no, diag=no, q_pipe=no, repair=no] sram_sp_1024x32
                   [SP=1_1_2, byp=no, diag=no, q_pipe=no, repair=no] sram_sp_1024x32
                   [SP=1_1_3, byp=no, diag=no, q_pipe=no, repair=no] sram_sp_1024x32
         [SEQ] # No.= 2,InstanceNo= 1,SEQ_max_addr_size= 24,Hier: top u_t1
             [GROUP] # No.=2_1
                   [2P=2_1_1, byp=no, diag=no, q_pipe=no, repair=no] rf_2p_24x28
         [SEQ] # No.= 3,InstanceNo= 1,SEQ_max_addr_size= 1024,Hier: top u_t1
             [GROUP] # No.=3_1
                   [DP=3_1_1, byp=no, diag=no, q_pipe=no, repair=no] sram_dp_1024x64

###Total mbist memory instance = 5
###Total SRAM/REGFILE = 3
###Total SRAM_2P = 1
###Total SRAM_DP = 1
###Total ROM = 0
###top_default algorithm is= (March C- @2P,SOLID)(March C-,SOLID)(March C+,SOLID)(March C- @DP,SOLID)

##################Not Group Memory List#########################################
```

Hierarchy

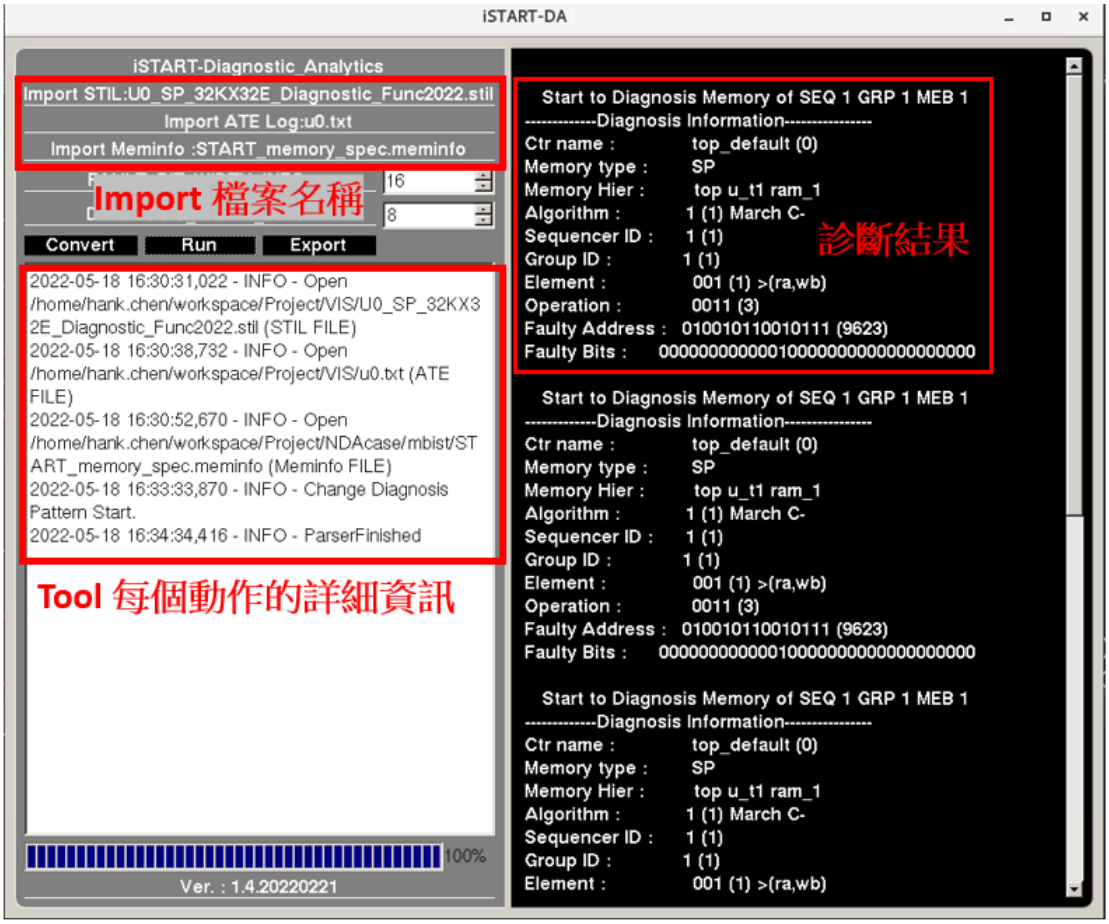
```
top u_t1 ram_1
top u_t1 ram_2
top u_t1 ram_3


top u_t1 u_2p


top u_t1 u_dp
```

Set FAULT_BIT_WIDTH and DAGNOSIS_WIDTH.

2. Convert: Perform conversion after importing all files.
   Run: Perform analysis after conversion.
   Export: Export the analysis result as a txt file.
3. Tool Execution Information: This section provides information and status updates for the tool execution
4. Progress Bar and Version Number
5. Tool Analysis Results: The tool's analysis result will be generated in this section.

Analysis Method: After importing all files and settings, the tool first analyzes the ATE result file and locate the faulty patterns. It then cross-references the STIL file to find and analyze the corresponding test commands. After analysis, it compares the memory order in the meminfo file and prints out the problematic memory information when exporting the result.

Analysis Result: The tool analysis is shown in the figure below. The right-hand block displays detailed information about the faulty memory, including the controller, memory type, memory hierarchy, and the information set in diagnosis_faulty_items of START™ v3.



圖中文字：

Import 檔案名稱→ The imported file names

Tool 每個動作的詳細資訊→Detailed information of each action of the tool

診斷結果→Diagnosis results

Authored by Hank Chen, Senior Engineer at iSTART-TEK

Year-End Tea Party

The COVID-19 pandemic has reduced the frequency of people's face-to-face interactions, but now, as we coexist with the virus, life is gradually returning to normal. iSTART-TEK appreciates our distinguished guests who attended our annual Year-End Tea Party held at the Sheraton Hsinchu Hotel. We enjoyed the time we spent together, celebrating the end of another successful year.

iSTART-TEK's Winter Course for TSRI

iSTART-TEK (TW: 6786), Asia's only EDA tool and IP provider of memory testing and repair solutions, has held a training course called "The Implementation of Built-in Self Testing Circuits in Embedded Memories of SoCs" in the 2023 winter vacation chip design class of Taiwan Semiconductor Research Institute (TSRI) at the National Applied Research Laboratories. The purpose of this course is to help the semiconductor industry cultivate chip design talents and establish a solid foundation in academic research.

Said by iSTART-TEK, the participants are majorly the students and professionals from well-known colleges and universities. Conducted by the senior R&D team of iSTART-TEK, his course contained the introduction and practice of EZ-BIST, an EDA tool powered by the company. The course offered a sequential curriculum design and support from the R&D team, allowing each participant to gain hands-on experience and a thorough understanding of the EZ-BIST operational process.

EZ-BIST memory testing circuit development environment is an GUI (Graphical User Interface) based EDA tool. It provides various built-in memory testing algorithms, allowing engineers to select the most suitable algorithms based on their chip development processes and applications. This tool facilitates implementation of memory testing algorithm circuits, and further shortens the time-to-market of the designed chips.

Webinar

iSTART-TEK provides a variety of automotive chip solutions and diagnostic tools that meet safety regulations. The Diagnosis ATE Tool enables chip developers to quickly and easily read memory error information from the ATE Log.