iSTART

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At a Glance: Why START™ v5 Stood Out at EE Awards Asia 2025

As SRAM becomes increasingly critical in advanced-node and AI-driven designs, test efficiency and flexibility are no longer optional—they are fundamental.

Recognized at the 2025, START™ v5 represents a new generation of SRAM test and repair solutions, built on patented MBIST algorithm technology and a highly flexible UDA modular framework.

By eliminating redundant test patterns and enabling customizable, process-aware test flows, START™ v5 helps IC design teams shorten test time, reduce manufacturing cost, improve coverage, and achieve higher yield with lower DPPM—without compromising reliability.

This industry recognition reflects a broader shift: memory test innovation is becoming a key enabler of advanced manufacturing success.

How Should We Respond to the New Compliance Challenges in the Automotive and Industrial Sectors?

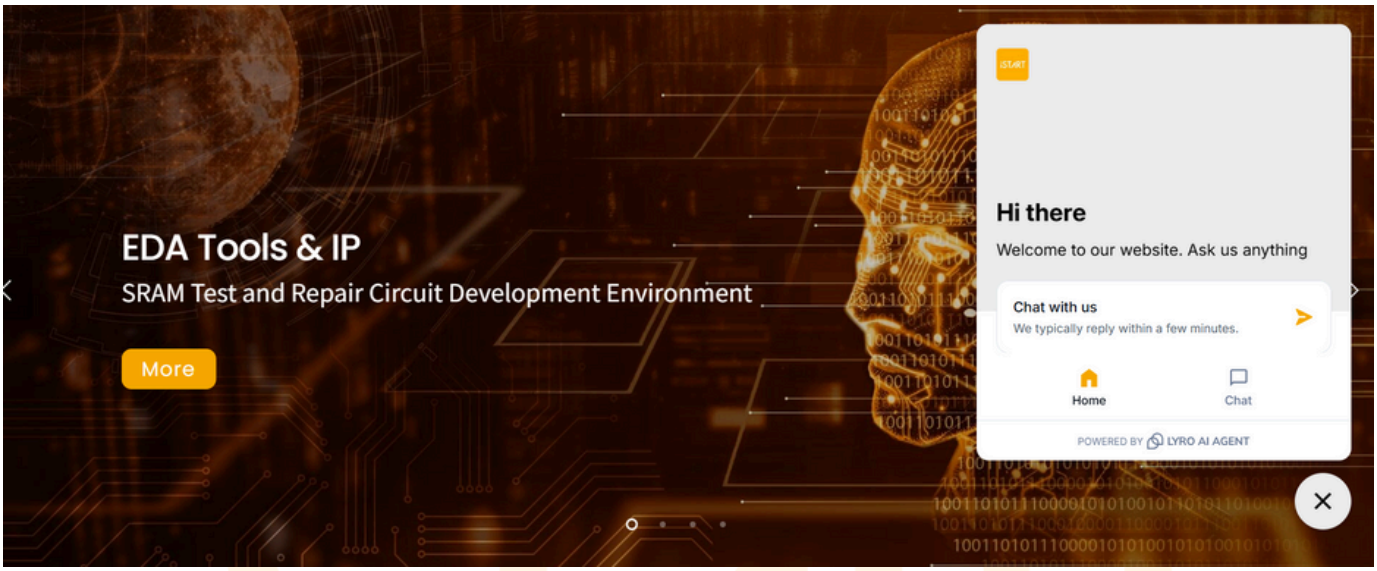
In the past decade, compliance requirements in the automotive and industrial sectors have increased rapidly. Multiple standards—including quality management, functional safety, cybersecurity, and information security—now operate concurrently, and semiconductor suppliers face challenges no longer limited to a single standard, but rather the complexity arising from overlapping requirements.

Although each standard has its own focus, they all revolve around core concepts such as risk management, process regulation, traceability, and evidence retention. In response to this trend, fragmented management approaches are no longer sufficient. Companies need to establish a unified compliance ecosystem that integrates the requirements of different standards, allowing the results of each implementation to reinforce one another. Compliance is no longer a one-time certification; it must be embedded throughout the product lifecycle and realized through engineering practice and continuous optimization. Engineers play a key role, needing to incorporate compliance thinking into design, development, and testing processes to mitigate risks from the outset and transform compliance into a competitive advantage.

In an environment where multiple standards run concurrently and compliance requirements continue to accumulate, the real challenge is not merely understanding regulations, but translating functional safety requirements into traceable and verifiable design and testing outcomes at the engineering level.

Facing these overlapping automotive and industrial compliance challenges, iSTART-TEK has consistently focused on helping customers implement functional safety. Our advanced EDA tools not only comply with ISO 26262 TCL1 standards but also actively perform FMEDA analysis, enabling engineers to establish complete and secure chip evidence during the design and testing phases, transforming compliance from a documentation requirement into verifiable engineering practice.

iSTART-TEK Continues to Optimize the Website's Interactive Experience with Its "AI Intelligent Instant Chat" Feature



iSTART-TEK's official website has officially launched the new AI smart instant chat feature, providing 24/7 intelligent interactive support to enhance user efficiency and convenience when browsing product information, accessing FAQs, or finding contact points.

The newly added AI chat function can instantly understand and respond to visitor inquiries, helping users obtain the information they need in the shortest time possible and reducing the wait for manual replies. With built-in Chinese and English language understanding, the system supports both local and international visitors.

The AI chat engine responds quickly to user questions and assists in locating product information, technical specifications, application details, and related documents. Through standardized answers and automatic page guidance, users can find the content they need without repeated searching or waiting, resulting in a smoother, clearer browsing experience and improved understanding of product structures and solutions, especially for first-time visitors.

To experience the new AI Smart Instant Chat feature, please visit the iSTART-TEK official website and click the "Chat with us" icon at the bottom right corner to start your conversation.

iSTART-TEK was Invited for an Interview at ICCAD, Showcasing Its Automotive-grade Memory Testing and Repair Capabilities

iSTART-TEK Featured in ICCAD Interview, Showcasing Leadership in Automotive-Grade Memory Test and Repair Technologies

During this year's Integrated Circuit Design and Application Conference & Exhibition (ICCAD), iSTART-TEK was invited for an exclusive interview with the semiconductor media outlet "ijiwei," where Ms. Nico Wang, the General Manager, and Mr. TP Hsieh, Deputy General Manager Shanghai iSTART-TEK Limited shared the company's core strengths in memory test and repair technologies.

Ms. Wang stated that iSTART-TEK specializes in MBIST and MBISR solutions, enabling chips to detect and repair memory defects before mass production, significantly improving yield and reliability. The company's proprietary EDA tools are now widely adopted across automotive, AI, HPC, networking, and consumer electronics markets, continuously expanding their technological impact.

Mr. Hsieh Manager highlighted that iSTART-TEK offers patented memory repair capabilities certified under ISO 26262 TCL1 and has independently completed FMEDA safety analysis, meeting the most stringent functional safety requirements for

automotive chips. In addition, iSTART-TEK's UDA + TEC platform helps customers customize SRAM test algorithms with the goal of reducing DPPM to zero. The newly launched AI tool, MART, can also recommend optimal test algorithms swiftly, greatly enhancing engineering efficiency. The company further provides comprehensive eFlash test and repair solutions with high coverage and strong repair capability to ensure superior chip quality.

During the exhibition, iSTART-TEK also prepared special giveaways and welcomed visitors to discuss technology trends and market needs at the booth. Through this interview exposure, iSTART-TEK once again demonstrated its leadership in memory test and repair technology and will continue to deliver innovative solutions that help customers build highly reliable chips.

SDMicro Adopts iSTART-TEK's START™ to Successfully Achieve Mass Production of 28nm Display Controller ICs

Sunrise Display Micro. (Suzhou) Co., Ltd. (SDMicro) has officially launched mass production of its latest 28nm display controller ICs, adopting iSTART-TEK's independently developed START™ v5 memory test and repair platform to ensure high reliability and yield during the production stage.

SDMicro, a display driver IC design company with proprietary intellectual property, focuses on the development of AMOLED display driver chips for popular applications such as smartphones and wearable devices.

In this project, SDMicro implemented several core features of the START™ v5 platform, including MBIST (Memory Built-In Self-Test), MBISR (Memory Built-In Self-Repair), UDA (User Defined Algorithm), and TEC (Test Element Change). By integrating customized SRAM test and repair designs, the team effectively enhanced memory test coverage and overall yield performance.

In display controller IC development, memory testing plays a critical role in determining product yield and stability. iSTART-TEK's START™ platform provides highly stable and comprehensive test coverage, enabling SDMicro to successfully complete mass production and achieve its targeted quality objectives.

TART™ v5 features a high-coverage memory test algorithm and a scalable repair architecture. The platform supports several key technologies, including:

- **MBIST + MBISR** – Rapidly locate and repair on-chip SRAM defects to significantly improve production yield.
- **TEC** – Coordinates the test control unit with external test interfaces, simplifying the mass production testing process.
- **UDA** – Enables customized test flows for various memory architectures, ensuring high coverage and low DPPM performance.

iSTART-TEK stated that SDMicro's successful mass production case demonstrates the proven effectiveness of the START™ platform in the display controller IC domain. Moving forward, the company will continue to drive broader collaboration to help customers achieve reliable high-volume production — with royalty contributions expected to begin next year.

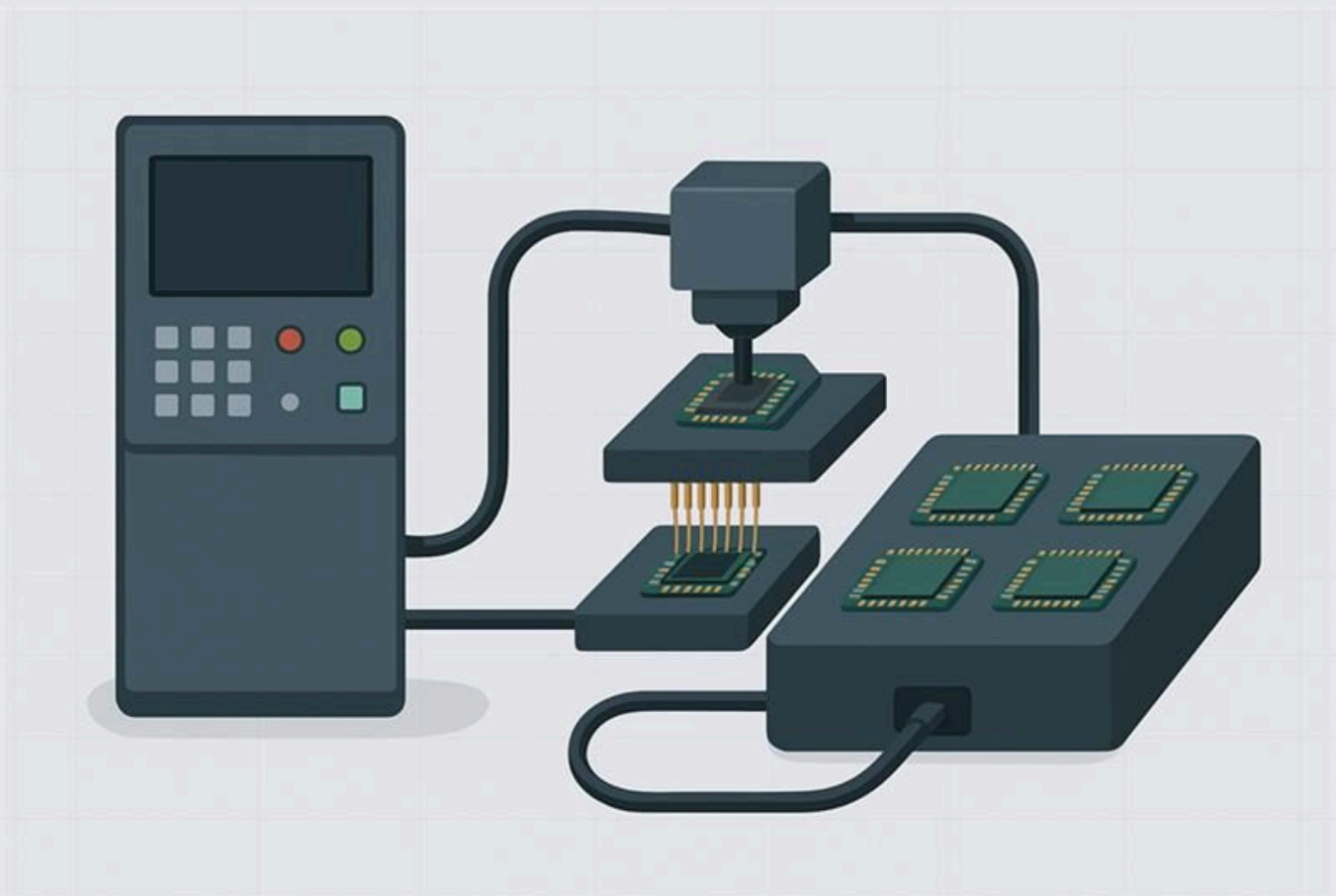
iSTART-TEK Brings Warmth Beyond Technology, Putting ESG Social Responsibility into Action

Focused on delivering advanced memory testing and repair solutions, iSTARK-TEK continues to create value for the semiconductor industry through innovative R&D while actively fulfilling its corporate social responsibility (ESG). On November 12, employees of iSTARK-TEK volunteered as caring companions, partnering with the Syin-Lu Social Welfare Foundation to accompany children in early intervention programs on a half-day outdoor activity. Through warm interactions and attentive companionship, the event brought joy to the children and created precious, lasting memories for everyone involved.

iSTARK-TEK emphasized that a company's value is reflected not only in its technical expertise and product performance, but also in its commitment to social contribution and responsibility. While striving to provide optimized memory testing and repair solutions, the company actively puts its ESG principles into practice by encouraging employee participation in charitable activities, extending care and compassion beyond professional expertise to give back to society.

Looking ahead, iSTARK-TEK will continue to promote diverse public welfare and social engagement initiatives, uniting corporate culture with the collective strength of its employees. By collaborating with social partners, the company aims to help build a more inclusive and supportive environment for the next generation—ensuring that technological advancement also serves as a force for warmth and positive impact in society.

Five Minutes to Understand ATE: the Unsung Hero Behind Semiconductor Mass Production Testing



After a chip completes design, manufacturing, and packaging, one critical step remains before it can officially ship — ATE testing. ATE, short for Automatic Test Equipment, is an indispensable tool in semiconductor mass production. Its role is to ensure that every IC meets specifications in functionality, electrical performance, and quality, preventing any potential defects from reaching the market.

The Role of ATE in the Semiconductor Production Flow

From design to shipment, an IC goes through four main phases: design, wafer fabrication, packaging, and testing. The testing phase is further divided into two steps:

Testing Stage	Target	Purpose
Wafer Sort	Bare dies on the wafer	Screens out defective dies to avoid easting packaging cost
Final Test	Packaged ICs	Verifies whether all functions and electrical characteristics meet specs

Both stages rely on ATE to perform automated operations. Using a probe card (during wafer sort) or test socket (during final test), ATE connects to the chip and simulates electrical signals under real operating conditions, checking its performance across different voltages, temperatures, and frequencies.

What Makes Up an ATE System

A complete ATE system typically consists of:

Module	Function
Tester	Provides power, clocks, and digital/analog signals
Handler / Prober	Automatically transports and positions chips
Test Program	Defines test items and pass/fail criteria
Load Board / Probe Card	Physical interface connecting the chip to the test system

During testing, the ATE outputs various signals based on predefined test programs and collects the chip's responses. Through high-speed measurement and comparison, the system quickly determines whether the chip passes the test. For complex ICs such as MCUs, SoCs, and memory devices, the ATE must support multi-channel operation, high-frequency signals, and large volumes of test vectors to ensure coverage and accuracy.

Why ATE Is Essential

In mass production, ATE is the first line of defense for quality, directly impacting overall yield and outgoing quality. Its main values include:

1. Ensuring correct functionality and preventing defective products from entering the market.
2. Monitoring process stability through test data and enabling early detection of abnormalities.
3. Reducing DPPM (Defective Parts Per Million) to meet the stringent requirements of automotive, industrial, and communication applications.
4. Enhancing production efficiency and reducing test cost through automation and data analytics.

For example, the DPPM requirement for automotive MCUs or memory ICs is often below 10 — meaning out of one million chips, no more than ten may be defective. Without high-performance ATE and rigorous test program design, achieving such a target is nearly impossible.

How iSTART-TEK Helps Improve ATE Test Efficiency

In ATE mass production, the test algorithm and test program are critical factors influencing coverage and efficiency. iSTART-TEK provides multiple test solutions for memory products that integrate seamlessly with ATE environments, including:

- **MBIST / eFlash BIST IP**: Built-in test logic that enables on-chip self-test, reducing ATE test time.
- **UDA + TEC Algorithm Generation Platform**: Automatically generates optimized test sequences based on the chip architecture and defect characteristics to improve test coverage.
- **Test Data Analytics Tools**: Integrates mass-production data to continuously refine test strategies and yield performance.

These solutions significantly enhance test efficiency and quality consistency without increasing ATE hardware load.

Conclusion

ATE is one of the most important components in semiconductor mass production testing and the final guardian of chip quality.
From wafer to finished product, ATE ensures each IC performs reliably across all application scenarios through fast and precise testing.
As chip technologies advance and test needs grow more complex, iSTART-TEK will continue delivering innovative BIST and algorithm-generation platforms to help customers achieve high coverage, high yield, and high reliability in ATE mass production environments.

Image Processing and Machine Vision: SRAM Testing and Repair

In image processing and machine vision applications—such as ISPs, industrial camera modules, and AI Vision SoCs—large volumes of embedded SRAM play a critical role in system performance and decision accuracy. Continuous read/write operations, multi-frame buffering, HDR processing, and AI feature-map movement all place heavy demands on SRAM stability. Even minor memory faults can directly manifest as image noise, distortion, or incorrect AI detection, ultimately impacting production quality and market reliability.

ChipStart Technology addresses these challenges with a comprehensive SRAM testing and repair solution tailored for high-speed access, long-term data retention, and harsh temperature conditions common in vision systems. By leveraging a flexible architecture combining Memory BIST, BIRA, and redundancy repair, potential memory defects can be detected and mitigated early in the design and manufacturing stages—effectively reducing DPPM, improving yield, and ensuring consistent product quality in mass production.

Key Advantages of the Solution

- **Effective DPPM Reduction**
- Weak bits, temperature-sensitive failures, and dynamic read/write faults are identified and contained before shipment, preventing issues from reaching end products.
- **Improved Production Yield**
- Row-, column-, and block-level redundancy repair preserves repairable dies, reducing unnecessary scrap and increasing overall manufacturing yield.
- **Support for High-Speed Imaging Workloads**
- Dynamic fault, coupling fault, and read-disturb testing ensure stable operation of high-frequency pixel and frame buffers.
- **Reliability for Long-Term Storage and AI Computation**
- Retention-aware test and repair strategies minimize data-loss risks in multi-frame stacking and AI feature-map storage.

- Designed for Automotive and Industrial Environments
- Extended voltage and temperature testing supports cold- and hot-boot scenarios, ensuring long-term reliability in harsh operating conditions.
- Optimized Test Efficiency and Cost
- Through algorithm flexibility and modular test architecture, high fault coverage is maintained while minimizing test time, reducing CP and manufacturing costs.

Building a Quality Advantage for Vision-System Mass Production

With a systematic SRAM test-and-repair flow, ChipStart Technology helps image processing and machine vision SoCs achieve predictable, stable quality during mass production. Beyond improving yield and reliability, the solution enables effective DPPM control and strengthens competitiveness across industrial vision, automotive imaging, and AI-driven visual markets.

▶ **Watch now**

Solving Small Memory Repair Challenges with the Repair Memory Wrapper

In memory-centric SoC designs, a large number of small SRAM instances are often used. If each memory block carries its own dedicated TRA (Testing Redundancy Analyzer) control logic, it results in duplicated circuits, routing congestion, higher area overhead, and increased power consumption. To address these challenges, iSTART-TEK introduces the Repair Memory Wrapper, a design approach that allows multiple memories to share a unified repair control logic, greatly improving efficiency and reducing architectural complexity.

The core advantage of the Repair Memory Wrapper lies in grouping multiple small memories—with identical functions and sizes—into one consolidated repair module. By sharing a single TRA, the design eliminates redundant logic, reduces area and power, and maintains full repair testability, while improving overall manageability within the SoC.

Users simply configure the wrapper parameters inside the User-Defined Memory (UDM). Once the UDM is imported into the iSTART EDA platform, the system automatically generates all required repair logic—no manual coding needed—making the workflow more intuitive and less prone to errors. During TRA operation, the system identifies which memory requires repair based on the incoming address and automatically routes the correct repair address and repair enable information to the corresponding ports, ensuring a precise and reliable repair process.

As advanced process technologies continue to impose stricter constraints on area and power, the Repair Memory Wrapper provides a more compact, efficient, and scalable repair architecture. It helps customers enhance yield, control DPPM, and improve overall SoC quality and competitiveness—making it a key technology for modern memory-intensive designs.

▶ **Watch now**

A Rare EDA Tool Achieving both TCL1 Certification and FMEDA Compliance – Safeguarding Functional Safety for Automotive ICs

Automotive semiconductors must maintain long-term reliability under extreme temperatures, vibration, and electrical stress, placing stringent requirements on IC functional safety and design robustness. With years of dedicated development in memory test and repair technologies, iSTART-TEK delivers patented EDA solutions engineered to meet the demanding standards of automotive-grade applications.

The START™ platform is certified under ISO 26262:2018 TCL1, and fully integrates FMEDA (Failure Modes, Effects, and Diagnostic Analysis) to help customers quantify risks, identify critical failure modes, and evaluate diagnostic coverage from the earliest stages of design—enhancing safety mechanisms and compliance readiness.

As one of the few vendors capable of offering both TCL1 certification and built-in FMEDA support, iSTART-TEK provides multiple key advantages for automotive semiconductor development:

- Strengthens functional safety credibility and enhances market competitiveness
- Shortens automotive project onboarding and accelerates time-to-market
- Supports ASIL-A through ASIL-D applications with comprehensive tool coverage
- Reduces regulatory risk and improves process consistency
- Integrates seamlessly with customers' functional safety and ASPICE workflows

Through a systematic safety-analysis framework and a fully compliant toolchain, iSTART-TEK enables customers to establish a complete functional-safety loop across design, testing, and mass production—delivering automotive ICs with higher reliability and long-term operational stability.

Watch now