iSTART

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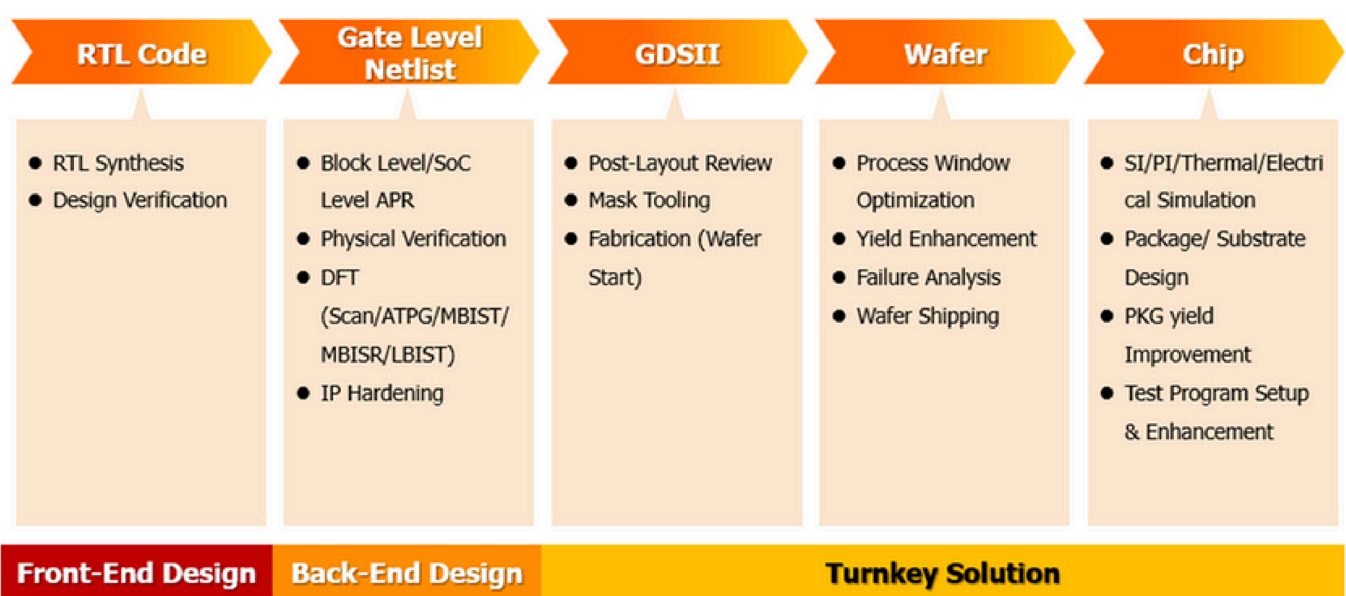
iSTART iReport

Issue No. 13

iSTART-TEK Successfully Assists a Leading Chip Design Company to Realize 55nm eFlash Chip Design Verification and Mass Production

iSTART-TEK announced that it has successfully assisted a well-known chip design company in China in completing its 55nm eFlash process chip design project. The collaboration covered the entire flow, from front-end IP evaluation and eFlash BIST IP design to back-end APR (Automatic Place and Route) and turnkey tape-out services, demonstrating iSTART-TEK's comprehensive capabilities in design services and process integration.

The partner company, a leading chip design firm focused on automotive and industrial safety applications, specializes in high-security MCU chips. In this project, iSTART-TEK leveraged its self-developed eFlash BIST IP to help the customer achieve high test coverage and process-compliant memory testing. By integrating a comprehensive IC design service platform—covering design verification, physical design, and mass production—iSTART-TEK provides a one-stop delivery capability that allows customers to focus on innovation in chip architecture and system applications.



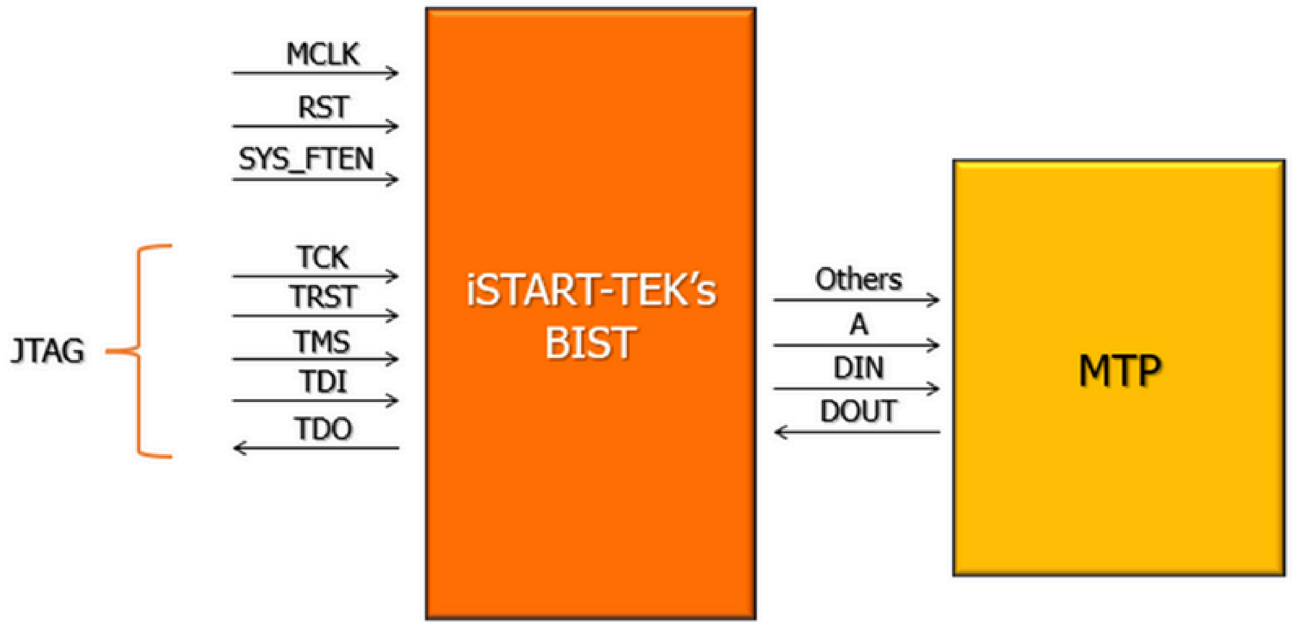
iSTART-TEK stated that this collaboration not only proves its strong technical expertise in eFlash process and BIST solutions but also reinforces its position in the high-reliability chip design service market. Moving forward, iSTART-TEK will continue to advance its memory test and repair technologies, expand to more process nodes and application domains, and help customers accelerate their time to market.

News

iSTART-TEK and a Leading Domestic Memory Manufacturer Successfully Verified MTP BIST IP

iSTART-TEK announced that its self-developed MTP (Multiple-Time Programmable) BIST IP has been successfully verified in collaboration with a leading domestic memory manufacturing company, and has passed the functional verification on a real test chip. The verification results show that iSTART-TEK's MTP BIST IP features high stability and flexible integration capability, and will be widely applied in various consumer electronic products in the future.

This verification was conducted using a 0.18 um logic process (1.8V/5V). The test chip includes a 16Kx16 main block and a 64x16x2 information block, with a total of 87 I/O pins. The MTP BIST IP uses a 5-pin JTAG interface to perform testing on the ATE platform, and supports the CP1 / CP2 test flow used in the manufacturing process, which can effectively detect potential defects in MTP memory cells. When the TF pin outputs 1'b1 during testing, a failure can be quickly identified, helping engineers to monitor yield conditions in real time.



At the system integration level, the MTP BIST IP allows adjustment of test flow parameters, flexibly supporting different SoC design requirements. It can also greatly shorten ATE test time and reduce test loading. Since MTP has the advantages of small area and low power consumption, when combined with iSTART-TEK's BIST IP, it enables customers to easily complete comprehensive memory test verification at the SoC design stage, improving product quality and production efficiency.

iSTART-TEK stated that, in addition to the verified MTP BIST IP, the company's complete NVM BIST IP product line, including eFlash BIST IP, has also been successfully verified on automotive and consumer IC platforms. The company expects these products to start contributing royalty revenue next year (2026), continuing to expand its market presence in the field of non-volatile memory testing.

News

iSTART-TEK EDA Products Fully Support IEEE 1838, Pioneering Innovation in 3D IC Memory Testing

iSTART-TEK announced that its memory testing solutions now fully support the IEEE 1838 standard interface, helping customers accelerate the testing and verification of 3D ICs.

While 3D ICs deliver higher performance and density, they also significantly increase the challenges and quality requirements of memory testing. To address these challenges, the IEEE 1838 standard establishes a comprehensive test mechanism—and iSTART-TEK has taken the lead in deploying this interface in practical memory testing.

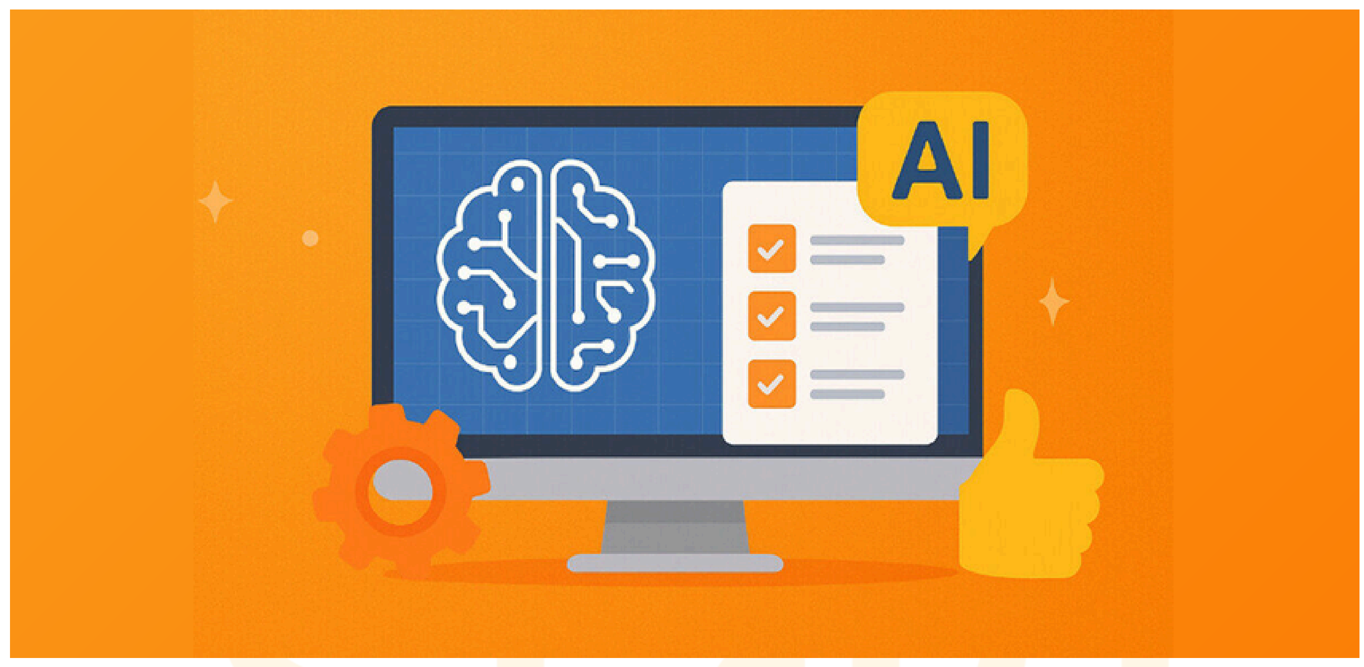
iSTART-TEK's solution enables each die to independently generate an MBIST (Memory Built-In Self-Test) circuit, which is then connected through standardized interfaces to shared I/O ports within a unified test architecture, allowing all dies to be tested.

This interface allows parallel memory testing of multiple dies simultaneously or independent testing of each die’s memory. Not only does this significantly reduce design complexity, but it also enhances flexibility for customer verification. More importantly, the architecture effectively increases test coverage, ensuring high standards of functionality and reliability for the chips.

iSTART-TEK emphasized that as 3D IC adoption grows rapidly, reliable testing solutions are critical to maintaining competitiveness. With IEEE 1838 support, its products not only simplify testing challenges in both design and production stages of 3D chips but also reduce testing risks, while delivering higher-quality chips for high-performance computing, AI, and automotive applications.

News

iSTART-TEK Unveils Industry-First AI-Powered MBIST Algorithm Recommendation Tool



iSTART-TEK announced the launch of an industry-first innovation—the MBIST Algorithm Recommendation Tool (MART)—which integrates AI technology into the existing UDA (User-Defined Algorithm) framework. With MART, users simply answer a set of interactive questions to quickly receive tailored recommendations for MBIST (Memory Built-In Self-Test) algorithms. The tool then automatically generates optimized BFL configuration files that can be directly applied to design and test flows, significantly enhancing both efficiency and accuracy.

Traditionally, when engineers develop test plans, it is usually just simple rule matching, which lacks flexibility; at the same time, they must rely on cumbersome table lookups and experiential judgment to select suitable test algorithms. However, as process nodes continue to evolve, application scenarios diversify, and requirements for quality and delivery schedules become stricter, these traditional methods can no longer meet the dual demands of speed and precision.

To address these challenges, iSTART-TEK has introduced the concept of AI-driven weighting. Each design factor—such as power, area, and yield—is assigned a weight, and AI dynamically adjusts these weights based on historical cases and its built-in knowledge base. The resulting algorithm recommendations are therefore not merely "rule matches," but optimal solutions derived from multi-factor weighted analysis.

The core values of MART include:

- Reduced decision cost: No more manual table lookups—AI automatically performs weighted analysis based on conditions.
- Smarter recommendations: Algorithm choices that better reflect the customer's real-world needs.
- Flexibility and control: Customers make the final decision, balancing AI insights with engineering expertise.

By leveraging AI weighting, MART not only improves MBIST efficiency but also helps customers strike a better balance between quality and performance in both design and production. It shortens early decision-making cycles and reduces DPPM (Defective Parts Per Million).
iSTART-TEK further stated that future expansions of MART will cover additional SRAM test modes and extend to logic testing, MBISR (Memory Built-In Self-Repair), and on-chip reliability analyzers—building a comprehensive, intelligent DFT (Design for Test) ecosystem.

iSTART-TEK Completes FMEDA Analysis to Help Customers Build ISO 26262-Compliant Automotive ICs

In response to increasingly stringent functional safety standards in automotive semiconductors, iSTART-TEK has proactively implemented FMEDA (Failure Modes, Effects, and Diagnostic Analysis) within its EDA tools. This supports the ISO 26262 standard process, enabling customer design teams to identify potential risks early in the development stage and strengthen both the safety and compliance of their designs.

ISO 26262 is an international functional safety standard for automotive electronic and electrical systems, covering hardware, software, and system-level development processes. For companies designing automotive ICs such as Advanced Driver Assistance Systems (ADAS), Electronic Control Units (ECUs), and Battery Management Systems (BMS), conducting systematic risk analysis in the early design phase is essential to meeting Automotive Safety Integrity Level (ASIL) requirements.

iSTART-TEK has observed that many automotive IC design companies face bottlenecks when introducing ISO 26262 processes due to the lack of tool-level support for functional safety analysis. To help customers deliver compliant products and accelerate time-to-market, iSTART-TEK has integrated FMEDA into its EDA tool suite. Key benefits include:

1. Enabling the development of ISO 26262-compliant products by supporting functional safety requirements within the design process.
2. Allowing customers to reference iSTART-TEK's FMEDA results to generate reliable FMEA reports without starting from scratch, significantly reducing the time needed to prepare safety assessment documentation.
3. Providing critical analytical support for achieving ASIL B/C/D systems when EDA tools include FMEDA analysis, thereby enhancing tool value.
4. Differentiating iSTART-TEK's tools from those without safety certification in the EDA market, delivering a distinct competitive advantage.

By integrating FMEDA into its EDA tools, iSTART-TEK not only helps customers accelerate ISO 26262 compliance but also improves the overall reliability of automotive IC design. This forward-looking strategy enables design teams to overcome functional safety bottlenecks, achieve ASIL certification, and deliver automotive chips that meet the highest safety standards.

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iSTART-TEK Selected as a Finalist for the 2025 EE Awards Asia – Product Award

iSTART-TEK's self-developed EDA tool, START™ v5 (SRAM Test and Repair Solution), has been successfully shortlisted for the 2025 EE Awards Asia in the EDA Product Category, competing alongside leading semiconductor and electronic design companies across Asia. This recognition highlights the innovation and global competitiveness of Taiwan's EDA technology.

Organized jointly by EE Times Asia and EDN Asia, the EE Awards Asia is one of the most prestigious and influential events in the electronics industry across the Asia-Pacific region. The award is determined through a combination of expert review and engineer voting, honoring companies and products that demonstrate outstanding innovation in electronic design, semiconductor technology, and application development.

iSTART-TEK's UDA (User-Defined Algorithm) platform is built on its patented technology, "Method for Generating a Memory Built-In Self-Test Algorithm Circuit," which breaks through the limitations of traditional memory test approaches. Conventional memory test algorithms often involve redundant testing sequences, resulting in longer test times and higher manufacturing costs. The UDA platform adopts a modular architecture, allowing engineers to flexibly edit test elements, eliminate redundancies, customize test flows, and optimize strategies for different processes and memory architectures. This significantly shortens test time, reduces DPPM, and enhances both test coverage and chip yield — providing a highly flexible and scalable solution for detecting memory defects in advanced process nodes.

After obtaining its Taiwan patent in 2022, this technology was further granted a U.S. patent in October 2023, marking a major milestone for iSTART-TEK's innovation and R&D excellence in global memory test technology. This recognition strengthens the company's confidence in helping customers tackle complex memory test challenges while improving design and production efficiency.

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News

iSTART-TEK Obtained U.S. Patent, “Configurable Testing and Repair System for Non-Volatile Memory”!

iSTART-TEK is proud to announce that we have been granted a U.S. invention patent for our “Configurable Testing and Repair System for Non-Volatile Memory”, reinforcing our leadership in advanced memory test and repair technologies.

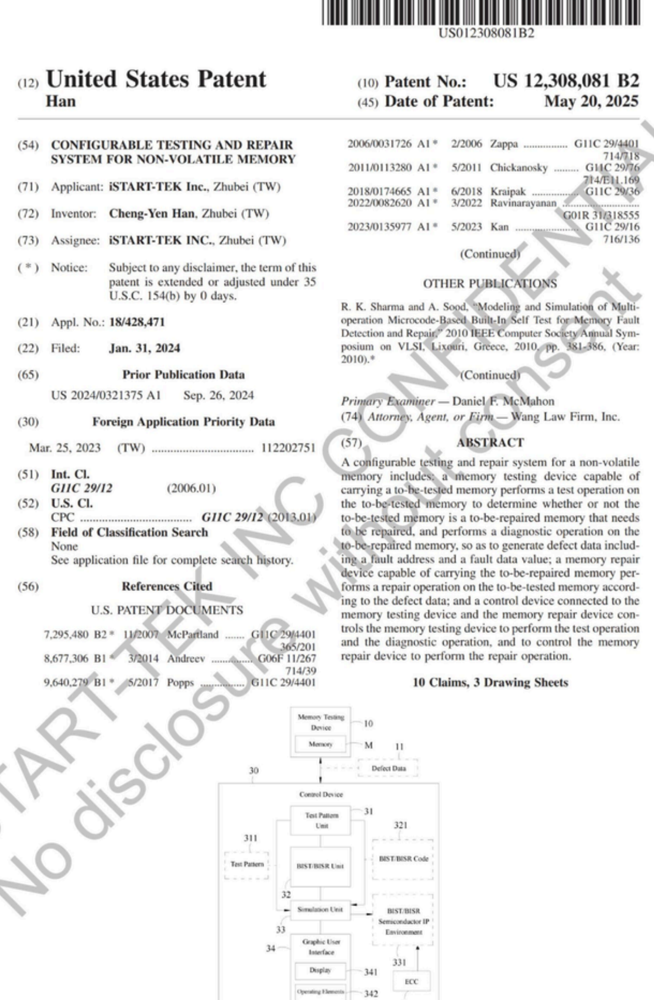
This patented system enables a configurable flow that includes:

📌 A memory testing device to determine whether a memory requires repair and to generate diagnostic defect data (fault address and fault value)

📌 A memory repair device that executes repair based on diagnostic results

📌 A control unit that orchestrates both testing and repair operations seamlessly

This innovation empowers iSTART-TEK to deliver more reliable, efficient, and flexible memory test solutions for our global partners.



US012308081B2

(12) **United States Patent**
Han

(10) **Patent No.: US 12,308,081 B2**
(45) **Date of Patent: May 20, 2025**

(54) **CONFIGURABLE TESTING AND REPAIR SYSTEM FOR NON-VOLATILE MEMORY**

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(72) Inventor: **Cheng-Yen Han**, Zhubei (TW)

(73) Assignee: **iSTART-TEK INC.**, Zhubei (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **18/428,471**

(22) Filed: **Jan. 31, 2024**

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(30) **Foreign Application Priority Data**

Mar. 25, 2023 (TW) 112202751

(51) **Int. Cl.**
G11C 29/12 (2006.01)

(52) **U.S. Cl.**
CPC *G11C 29/12* (2013.01)

(58) **Field of Classification Search**
None
See application file for complete search history.

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(Continued)

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(57) **ABSTRACT**

A configurable testing and repair system for a non-volatile memory includes: a memory testing device capable of carrying a to-be-tested memory performs a test operation on the to-be-tested memory to determine whether or not the to-be-tested memory is a to-be-repaired memory that needs to be repaired, and performs a diagnostic operation on the to-be-repaired memory, so as to generate defect data including a fault address and a fault data value; a memory repair device capable of carrying the to-be-repaired memory performs a repair operation on the to-be-tested memory according to the defect data; and a control device connected to the memory testing device and the memory repair device controls the memory testing device to perform the test operation and the diagnostic operation, and to control the memory repair device to perform the repair operation.

10 Claims, 3 Drawing Sheets

iSTART-TEK INC CONFIDENTIAL
No disclosure without consent

USB Type-C: The Universal Interface for Modern Electronics

USB Type-C has become the standard interface across modern electronic devices—from smartphones and laptops to automotive systems, medical equipment, and industrial controllers.

It is more than just a reversible connector shape; it is a comprehensive interface and communication standard that supports high-speed data transfer, high-power charging, and the integration of video and data signals. Its introduction has simplified product design and accelerated the unification and interoperability among different electronic devices.

Key Features of USB Type-C

1. Reversible Design

The Type-C connector features a symmetrical design, allowing it to be plugged in either way, improving user convenience and durability.

2. High-Speed Data and High-Power Delivery

USB Type-C supports the USB 3.2, USB4, and even Thunderbolt 4 standards, enabling data transfer rates of up to 40 Gbps. Through the USB Power Delivery (PD) protocol, it can deliver up to 240W of power, allowing a single cable to handle both power and data transmission efficiently.

3. Multi-Function Integration

Beyond power and data transmission, Type-C can carry DisplayPort Alt Mode or HDMI Alt Mode signals, enabling laptops or tablets to connect directly to external displays, projectors, or cameras.

The table below summarizes the applications and key functions of USB Type-C in different domains.

Application Domain	Example Applications	Key Functions
Smartphones, Laptops	Charging and data transfer, single-port laptop charging, docking stations, external displays	High-power charging (PD), high-speed data transfer, video output (DP Alt Mode)
Automotive (Automotive-Grade)	Infotainment systems, in-car charging ports, digital dashboards	High reliability, power and data integration, compliance with AEC-Q100 automotive standards
Medical and Industrial Equipment	Medical imaging systems, industrial PCs (IPC), human-machine interfaces (HMI)	High stability and reliability, minimizing risk of system failure
Others	Monitors, external drives, printers, game consoles, cordless vacuum cleaners, and power tools	Single-cable solution for all charging and data needs, becoming a universal connectivity standard

Importance of Type-C in Automotive and Industrial Applications

In automotive, medical, and industrial environments, components must remain stable under high temperature, vibration, and long-term operation. For this reason, Type-C interfaces used in automotive-grade products must comply with rigorous standards such as AEC-Q100 or IATF 16949 to ensure reliability and safety.

For example, an in-car Type-C charging port may look ordinary, but it must withstand frequent plug-in cycles, high cabin temperatures, and voltage fluctuations—all while maintaining stable data communication with the vehicle system. These requirements rely on robust electronic design and thorough testing validation.

How iSTART-TEK Supports Type-C Related IC Testing

USB Type-C–related ICs, such as power management ICs, interface bridge ICs, and signal switch ICs, must undergo stringent electrical and reliability testing. iSTART-TEK provides comprehensive MBIST, eFlash BIST, and automotive-grade test solutions for high-speed interface and power management ICs, helping customers ensure consistent performance under high-speed transmission and high-power operating conditions.

Extended Reading: How MBIST and MBISR Safeguard USB Type-C Controller Chips

How MBIST and MBISR Safeguard USB Type-C Controller Chips

DThe USB Type-C interface has become a core feature in modern electronics — from smartphones and laptops to automobiles and medical devices. With its reversible plug design, high-speed data transfer, and power delivery capabilities, USB Type-C integrates multiple functions into a single, compact connector. However, this high level of integration also increases design complexity and manufacturing risks. Without comprehensive testing before shipment, it's difficult to guarantee that a chip will perform reliably under demanding conditions. This is where MBIST (Memory Built-In Self-Test) and MBISR (Memory Built-In Self-Repair) come in.

In this episode of iSTART Class, we explore how MBIST and MBISR protect USB Type-C controller chips from potential memory and logic faults. At the module level, MBIST has become an essential part of self-testing digital logic, while MBISR provides fault-tolerant repair when SRAM or other repairable resources are involved. Together, they form a robust defense that ensures both cost efficiency and long-term reliability.

From a broader market perspective, the requirements for testing and repair vary across applications. Consumer electronics prioritize cost-effectiveness and basic MBIST coverage, while industrial and medical systems demand higher stability and extended test coverage. In contrast, automotive-grade chips must fully comply with the AEC-Q100 standard, requiring comprehensive MBIST and MBISR mechanisms to withstand extreme temperatures, vibration, and electrical stress. Through a well-structured test and repair flow — from self-test activation to automatic defect repair and re-verification — USB Type-C controller chips can self-classify during mass production, preserving yield and ensuring reliability.

Backed by ChipStart's expertise in memory testing and repair technologies, our solutions, including UDA (User-Defined Architecture) and TEC (Test Engine Controller), help customers customize their MBIST and MBISR implementations for maximum performance and manufacturability. From IP-level support to full SoC integration, ChipStart empowers designers to achieve optimal quality and faster time-to-market.

▶️ **Watch now**

Networking ASIC and SRAM Test & Repair

To support high bandwidth and low latency, networking chips often embed large, multi-block SRAM for critical functions such as switch buffers, packet scheduling tables, and flow entry tables. However, these memories are highly susceptible to process variation. Even if one memory block fails, overall chip yield may remain high. That's where BIST (Built-In Self-Test) and BISR (Built-In Self-Repair) come in—enabling quick fault detection and repair through spare rows, columns, or blocks, without scrapping the entire chip.

In this video, we'll cover:

- Real-world use cases in Wi-Fi 7 SoCs, Switch ICs, SerDes/PCIe PHY, and 5G Modems
- How BIST ensures coverage while BISR isolates and repairs defective memory cells
- Additional modules such as Logic BIST and On-chip Repair Analyzer for unified test & repair flow
- How these solutions improve yield, reliability, and DPPM while supporting long-term operation

With BIST and BISR working hand-in-hand—plus support for OTA, Field Repair, and Post-Silicon Repair—Networking ASICs can achieve carrier-grade reliability, maintain throughput in real-world conditions, and extend product lifetime.

▶️ **Watch now**

Why Do Bluetooth Chips Need SRAM Test Algorithms?

Although Bluetooth chips are small and low-power, they integrate multiple SRAM blocks that store packets, communication buffers, and control information. The stability of these SRAMs directly affects the chip's communication quality and overall system functionality. The main reasons why SRAM testing is important include:

- Embedded SRAM is a critical component
- Yield verification is required during package testing
- Sensitive to power and process variations
- SRAM is located in low-power islands

iSTART-TEK's SRAM Testing Solution for BLE Chips

To address these challenges, iSTART-TEK has developed testing and repair strategies specifically for low-power Bluetooth chips:

- Retention-aware March algorithms
- Pattern Generator + Fault Simulator
- Built-in Repair Logic

Application Scenarios

- **Wearable devices (e.g., smart bands)**: High demands due to space constraints and high integration; even minor failures pose risks.
- **Automotive Bluetooth modules:** Must comply with AEC-Q100, with clear requirements for SRAM testing and reliability.
- **IoT sensors:** Long operating times and low-power requirements make Retention Fault detection especially critical.

Although BLE chips are small, their SRAM stability requirements are very high. Introducing advanced testing and repair mechanisms from the design stage not only improves yield but also enhances the end product's user experience and reliability.

From Earphones to Automotive SoCs: Practical SRAM Repair Techniques for Audio Applications

In audio chip design, SRAM serves as the core component of the data buffer, responsible for storing intermediate data generated during audio processing, such as filter states, FFT data, and echo parameters.
If a defect occurs in the SRAM, it may lead to audio distortion, noise, or even system crashes. As a result, more and more audio products—including headphones, hearing aids, and voice-controlled devices—are incorporating SRAM repair technologies to ensure a stable and high-quality user experience.

Why Do Audio Chips Need SRAM Repair?

- **Prevent audio glitches and system crashes**
  Defective SRAM can directly affect sound output quality, causing minor issues like noise or major failures such as device reboots.
- **Address defect risks from advanced process nodes**
  As process technologies move below 28nm, the defect rate in SRAM increases. Even consumer-grade chips need built-in fault tolerance to maintain yield.
- **Enhance data retention in low-power devices**
  Audio chips often operate in sleep modes or face frequent power cycles. If the SRAM fails to retain data properly, so-called retention issues may occur, affecting device reliability at startup.
- **Improve overall chip yield and shipment stability**
  By integrating repair mechanisms, minor SRAM defects can be bypassed through redundancy, preventing entire chips from being scrapped and boosting the number of functional dies per wafer.

Common Application Scenarios

- **TWS Wireless Earbuds Chips**
  Simple repair mechanisms help prevent post-shipment issues like abnormal noise or system crashes.
- **Hearing Aid Chips**
  Due to frequent transitions to low-power states, retention testing and repair capabilities are especially critical.
- **Automotive Audio SoCs**
  To comply with reliability standards such as AEC-Q100, comprehensive SRAM repair and fault tolerance are required.

Recommended Repair Strategies by Application

- **Consumer Audio ICs**
  Basic redundancy mechanisms can enhance both stability and yield.
- **Automotive Audio Chips**
  Use of multi-level fault tolerance and error correction is recommended to ensure high reliability.
- **Low-power Portable Devices**
  Retention-aware repair solutions are advised to maintain data integrity.
- **Voice AI Chips**
  Integration of self-test and dynamic repair mechanisms is recommended to meet high-speed and complex computation demands.

With the right SRAM repair technologies, audio chips can significantly improve product yield and shipment stability. More importantly, they provide a solid foundation for reliable system performance—essential for meeting the demands of advanced processes and competitive markets.

▶️ Watch now

The Relationship Between Audio Processing and SRAM Test Algorithms

In audio application scenarios that demand high real-time performance and data accuracy, memory stability is increasingly becoming a critical aspect during both the design and testing phases.
The relationship between audio processing and SRAM testing algorithms highlights why, even though audio systems do not fall within traditional high-reliability domains, they impose equally stringent — and sometimes even more demanding — requirements on SRAM performance.

Key Highlights of This Episode:
Application Background & Technical Demands

- Common audio system functions such as noise reduction, decoding, and echo cancellation rely heavily on SRAM for high-speed data buffering and computation.
- The high-frequency and continuous data read/write operations expose potential risks in SRAM related to data retention and sustained access.
- Furthermore, the working environments of mobile devices — such as high temperatures and voltage fluctuations — present additional challenges to SRAM reliability.

Corresponding Strategies in Test Algorithms
This episode discusses algorithm design directions tailored to the specific characteristics of audio applications, including:

- **Retention-Aware March Test**
  Introducing delay cycles to simulate data dwell time, improving the detection of retention faults. This is especially suitable for low-power audio devices (e.g., earbuds, hearing aids).

- **At-Speed March Read-Write**
  Simulates real-world buffer behavior at operational frequency, effectively uncovering fault types that occur only under high-speed operation (e.g., transition faults, coupling faults).
- **Data Pattern Sensitivity**
  Utilizes common audio data patterns (such as interleaved 1010/0101) for testing to improve the detection rate of pattern-sensitive faults.

Application Insights & Design Recommendations

- Testing strategies should be enhanced to address continuous high-speed access and data retention capabilities.
- Test scenarios should reflect practical audio processing use cases — for example, focusing on "read-heavy, write-light" behavior and "low-latency, high-frequency response" in the test flow design.
- The User Defined Algorithm (UDA) platform offers highly flexible configuration capabilities, enabling engineering teams to optimize test structures according to specific application requirements.

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SRAM Testing Algorithm for Automotive-Grade Chips Part 3: Using UDA + TEC to Generate a Full-Coverage SRAM Defect Testing Algorithm

With the continuous adoption of advanced semiconductor processes like FinFET and GAA, while chip performance improves, the defect types of SRAM have also become more complex. New types of faults, such as Marginal Faults, Dynamic Faults, and even Soft Errors, are emerging—similar to how viruses mutate. Traditional March C testing algorithms are like "old vaccines": they may still be effective against some known defects, but they fall short when it comes to these "virus mutations."

To tackle this challenge, iSTART-TEK offers the UDA (User-Defined Algorithm) mechanism. Simply put, it works like a vaccine development platform, allowing customized testing algorithms to be tailored according to the characteristics and usage scenarios of the product. For example, if a product needs to operate in high-temperature environments, where leakage defects are more likely to occur, users can design algorithms with specific test patterns targeting such defects. It's like administering targeted vaccines to high-risk areas for enhanced protection.

In summary, the combination of UDA and TEC forms a tailor-made, comprehensive vaccine program for SRAM. As processes and application requirements continue to evolve, only by continuously updating testing algorithms can we guard against emerging defects, ensuring reliability and quality in critical fields such as automotive, AI, and aerospace.

▶ Watch now