Technical white paper of the highly configurable eFlash IP testing and epairing circuits development environment: EZ-NBIST

1. Testing methodologies of NVM IP

The testing methodologies of eFlash IP covers full wafer sort, and final test for

UMC's 40nm, 55nm and SST's 0.11um, 0.18um and customized embedded eFlash IP.

iSTART-TEK develops EZ-NBIST GUI tool to save BIST coding time of NVM IP.

EZ-NBIST follows eFlash vendor's testing methodologies to implement all test items' timing diagrams and save parallel long testing time in ATE.

2. Why NVM IP needs to use BIST and BISR?

NVM IP has complicated testing functions to cover each disturbing condition.

The memory BIST adds logic to an IC which allows the SoC to test its own memory operation.

MBIST tests the eFlash macro through an effective test algorithm to detect possibly all the faults. MBIST generates test patterns from eFlash vendor requirement to the eFlash macro and reads them to find any eFlash defects.

BISR adds repair circuit to backup memory to increase the eFlash IC yield.

3. How iSTART-TEK accomplish BIST and BISR of NVM IP?

iSTART-TEK develops EZ-NBIST GUI tool to generate BIST and BISR of eflash IP.

iSTART-TEK BIST implements all eFlash test items to cover wafer soft and final test. BIST interface is a flexible serial interface to reduce IC test pins. Increase BIST test flexibility, all test items can be enabled and disabled individually. Provide diagnosis mode to debug defect address.

iSTART-TEK BISR records eFlash faulty memory address and use redundancy sectors to increase eFlash IC yield. Provide auto repair function.

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Figure 1 shows eFlash test and repair solutions.

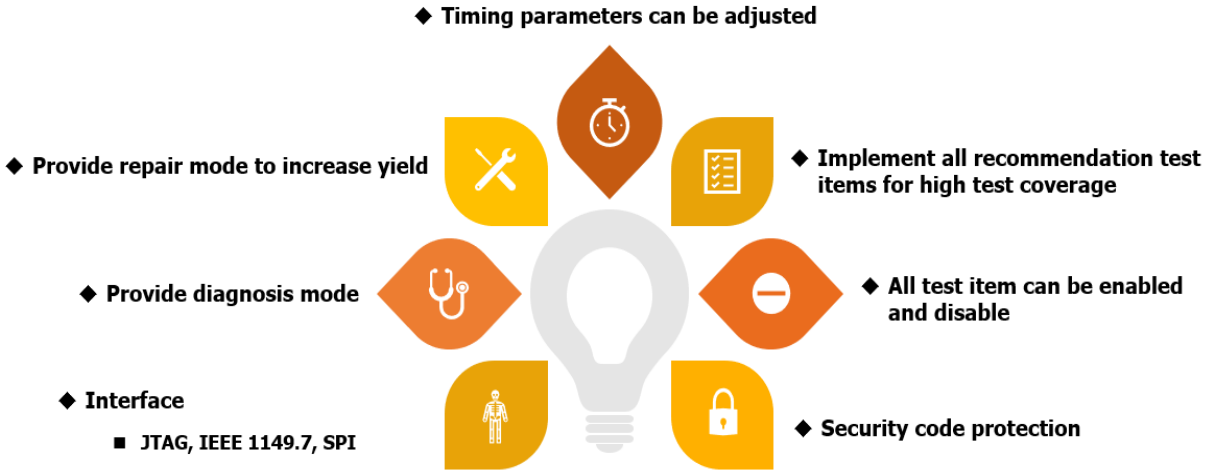

Figure 1

Figure 2 shows eFlash test and repair features.

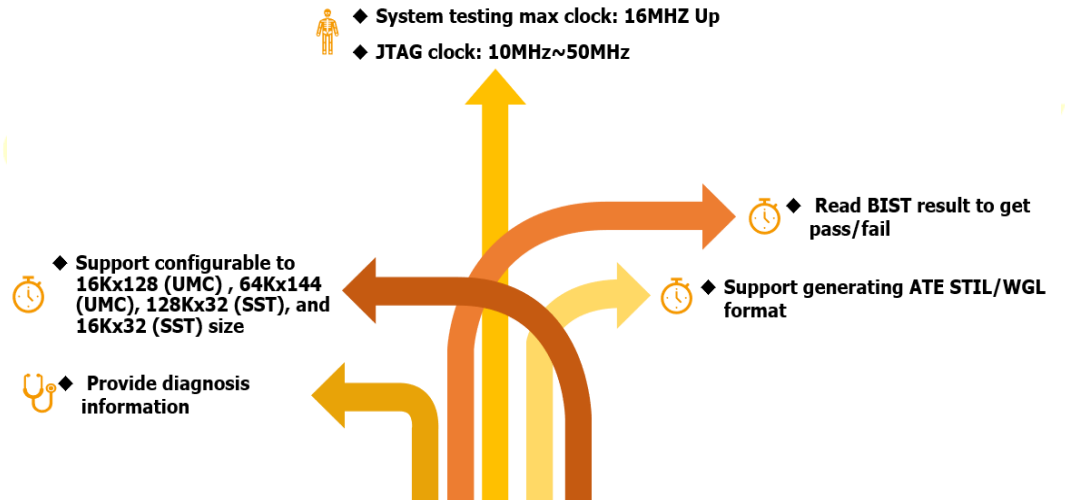

Figure 2

Figure 3 shows eFalsh diagnosis simulation output.

```
item cnt: 374
addr:     1
fault_bit:00000000000000000000010000000000

item cnt: 374
addr:   255
fault_bit:00000000000000000000010000000000

item cnt: 374
addr:   511
fault_bit:00000000000000000000010000000000

item cnt: 374
addr:   521
fault_bit:00000000000000000000010000000000

item cnt: 374
addr:   541
fault_bit:00000000000000000000010000000000
```

Figure 3

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Figure 4 shows BISR circuit block.

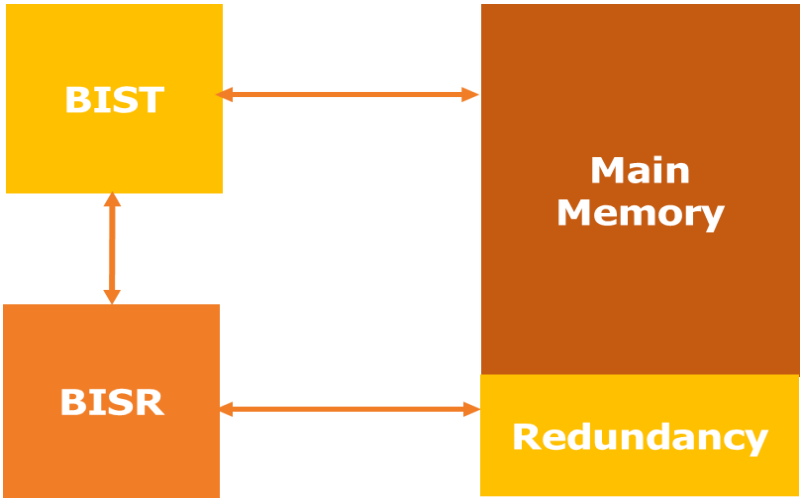

Figure 4

4. What is EZ-NBIST?

EZ-NBIST is an NVM GUI tool to generate BIST and BISR of NVM IP.

錯誤! 找不到參照來源。 shows the perspective of EZ-NBIST GUI. Click "EZ-NBIST Config" from "Config"

drop-down menu.

Figure 5

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Users click "Run…" from "Run" drop-down menu to execute EZ-NBIST.

Figure 6

5. How many NVM IP are included in EZ-NBIST?

EZ-NBIST GUI supports following eFlash IP for UMC 64Kx144, UMC 16Kx128, SST 128Kx32, SST 16Kx32 IP sizes and customized IP sizes.

Users can choose UMC, SST and customized eFlash macro types, vendor types and specific eFlash macro sizes as shown in Figure and Figure .

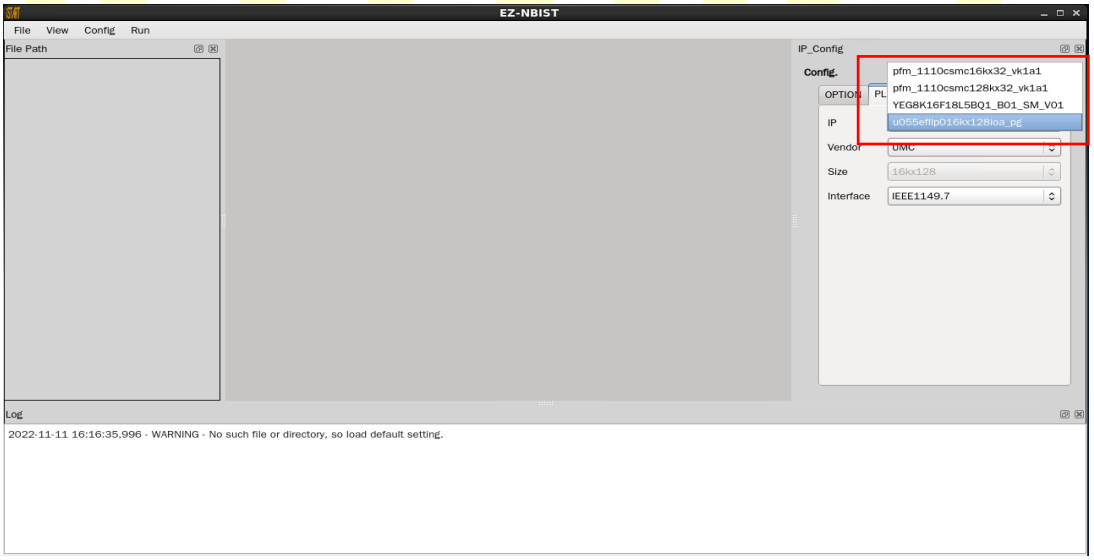

Figure 7

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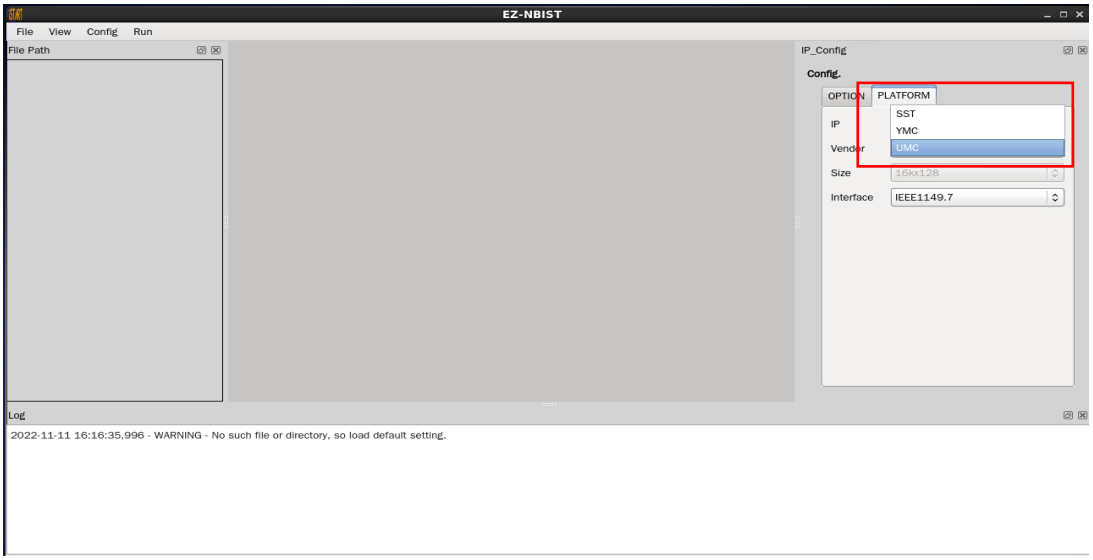

Figure 8

6. What kinds of interface are included in EZ-NBIST?

EZ-NBIST GUI supports 3 flexible serial interfaces JTAG, IEEE1149.7, and SPI as shown in Figure 9.

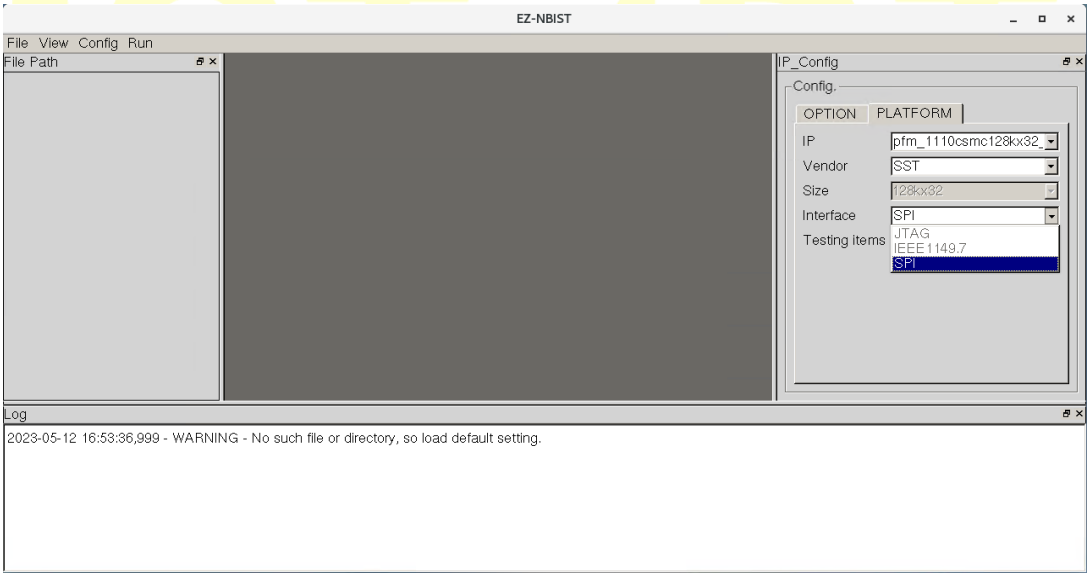

Figure 9

Figure 10 shows eFlash test and repair block with JTAG interface.

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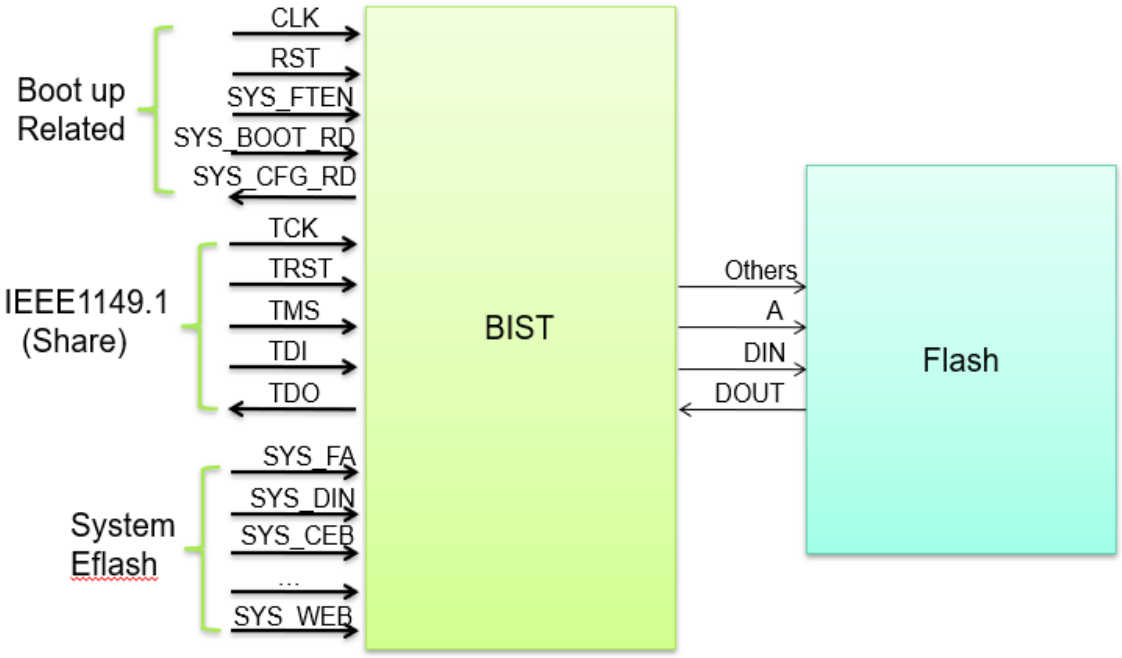

Figure 10

Figure 11 shows eFlash test and repair block with IEEE1149.7 interface.

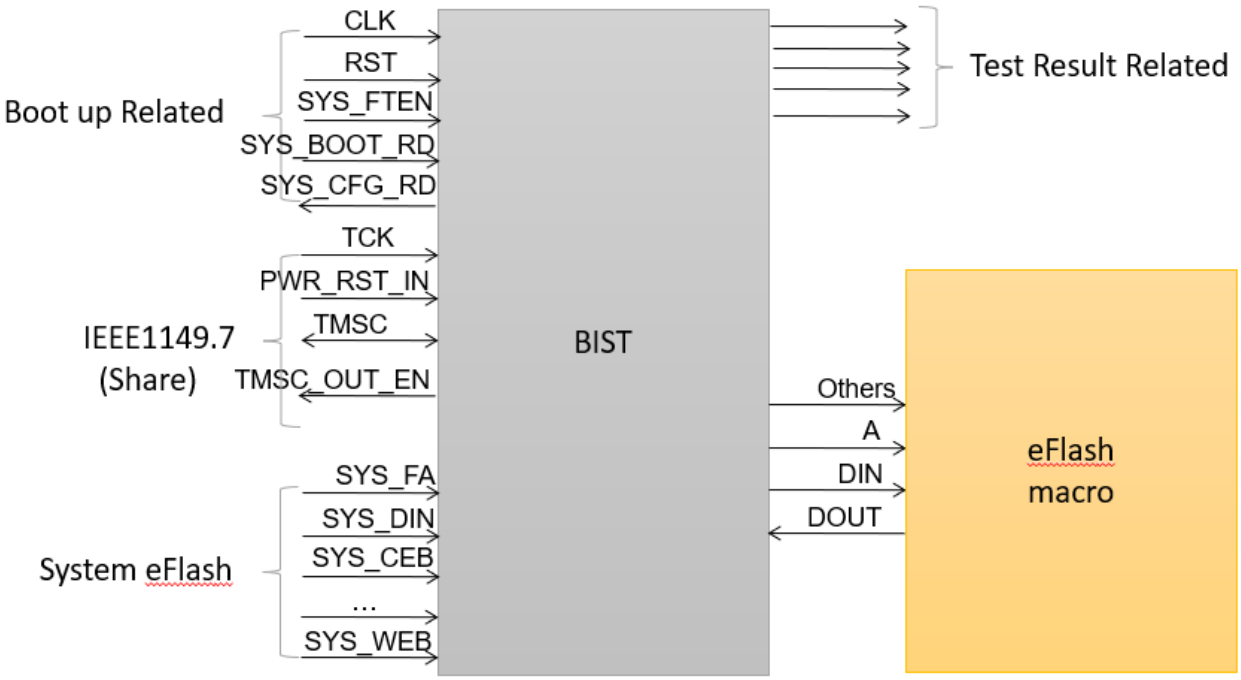

Figure 11

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Figure 12 shows eFlash test and repair block with SPI interface.

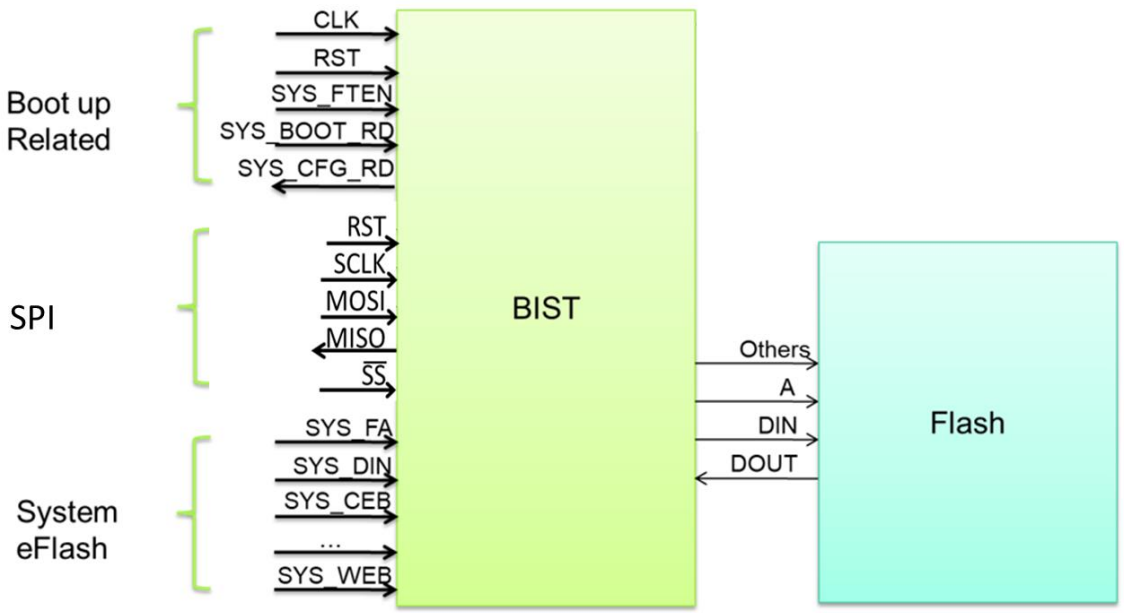

Figure 12

7. How flexibility of EZ-NBIST?

EZ-NBIST supports configurable BIST and BISR IP for different eFlash macro sizes. All eFlash timing parameters can be adjusted. Figure 13 shows all test items can be enabled and disabled individually.

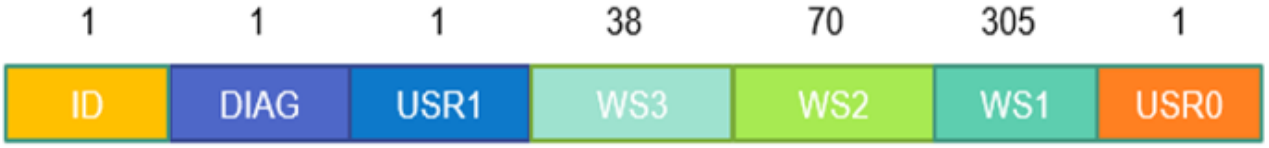

Figure 13

EZ-NBIST can help users to generate the complete synthesis RTL, the verification environment, the testing patterns, the behavior model, and the customized eFlash database as shown in Figure 14.

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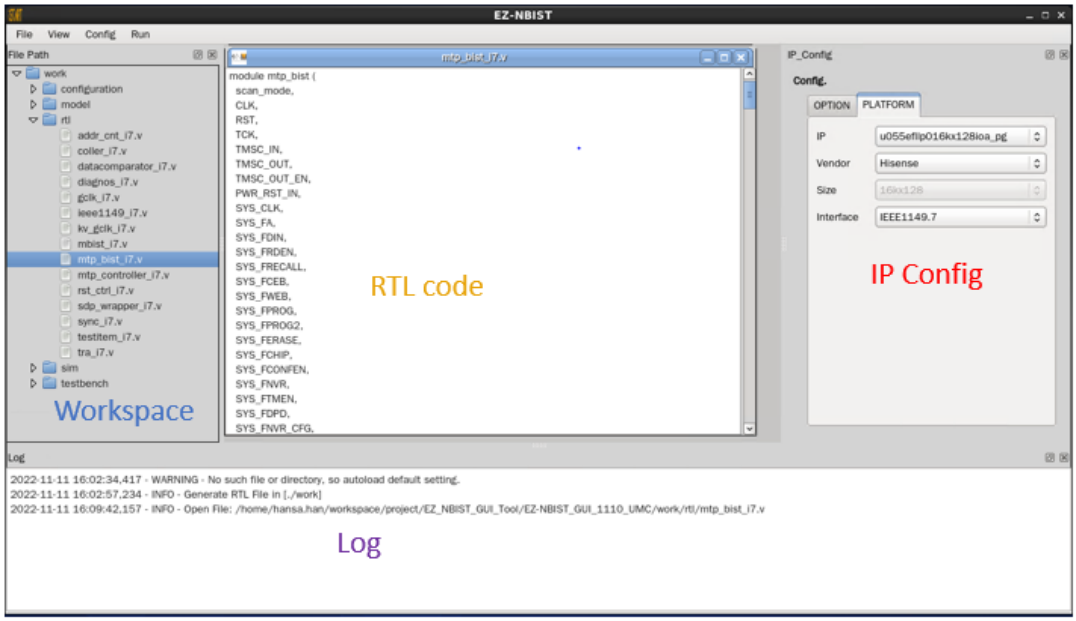

Figure 14

To execute simulation with eFlash model, users can select a test pattern to generate simulation dump files. For example, execute "2" in

```
1  1149         check dr1=10..01, dr2=2, dr3=3, dr4, ten= 1,0,1,1,0,0,1
                check tdo=10'b10_0000_0001 when ir=5
                check tdo=32'hffff_ffff when ir=6
                check clear_ten and ten
2  ws1          check ws1 test item
3  ws2          check ws2 test item
4  ws3          check ws3 test item
5  ws1_trim     check ws1 trim function
6  ws1_repair   check ws1 repair function
7  repair       check ws2 test item, has_fault
8  repair_fail  check ws2 test item, has_fault
9  diagnosis    check ws2 test item, has_fault
10 normal_test  check normal function
```

Figure 1 to start "ws1" testing item's simulation flow.

```
1  1149         check dr1=10..01, dr2=2, dr3=3, dr4, ten= 1,0,1,1,0,0,1
                check tdo=10'b10_0000_0001 when ir=5
                check tdo=32'hffff_ffff when ir=6
                check clear_ten and ten
2  ws1          check ws1 test item
3  ws2          check ws2 test item
4  ws3          check ws3 test item
5  ws1_trim     check ws1 trim function
6  ws1_repair   check ws1 repair function
7  repair       check ws2 test item, has_fault
8  repair_fail  check ws2 test item, has_fault
9  diagnosis    check ws2 test item, has_fault
10 normal_test  check normal function
```

Figure 1

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8.Conclusion

EZ-NBIST provides UMC and SST eFlash BIST/BISR with professional testing items. EZ-NBIST saves eFlash tuning parameter timing time in ATE. The eFlash BIST and BISR area overhead of SoC is acceptable. EZ-NBIST is also easy to set for accomplishing eFlash IP's testing circuit.

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