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EZ-BIST

An Easy-to-use EDA Tool

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EZ-BIST Features

◆**EZ-BIST** features simple setting and easy to use, suitable for developing MCU system which memory instances are less than 50. It is also the best tool for academic and semiconductor research institutions to realize MBIST behavior and implementation.

◆EZ-BIST's friendly interface and simplify operation enables users to build BIST circuit instantly, effectively shorten SoC development time, further improves product inspection and reduces development cost.

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EZ-BIST Features

- ◆Complete GUI interface
- ◆Support UDM (User Defined Memory)
- ◆Support memory grouping setting
- ◆Support auto clock tracing
- ◆Support clicks and drags to memory port insertion
- ◆Support gate-cell insertion for power saving
- ◆Smart error proofing design
- ◆BIST insertion supports up to 50 memory instances
- ◆Support multiple memory testing algorithms in MBIST design
- ◆Support testing algorithms selection via application & technology node

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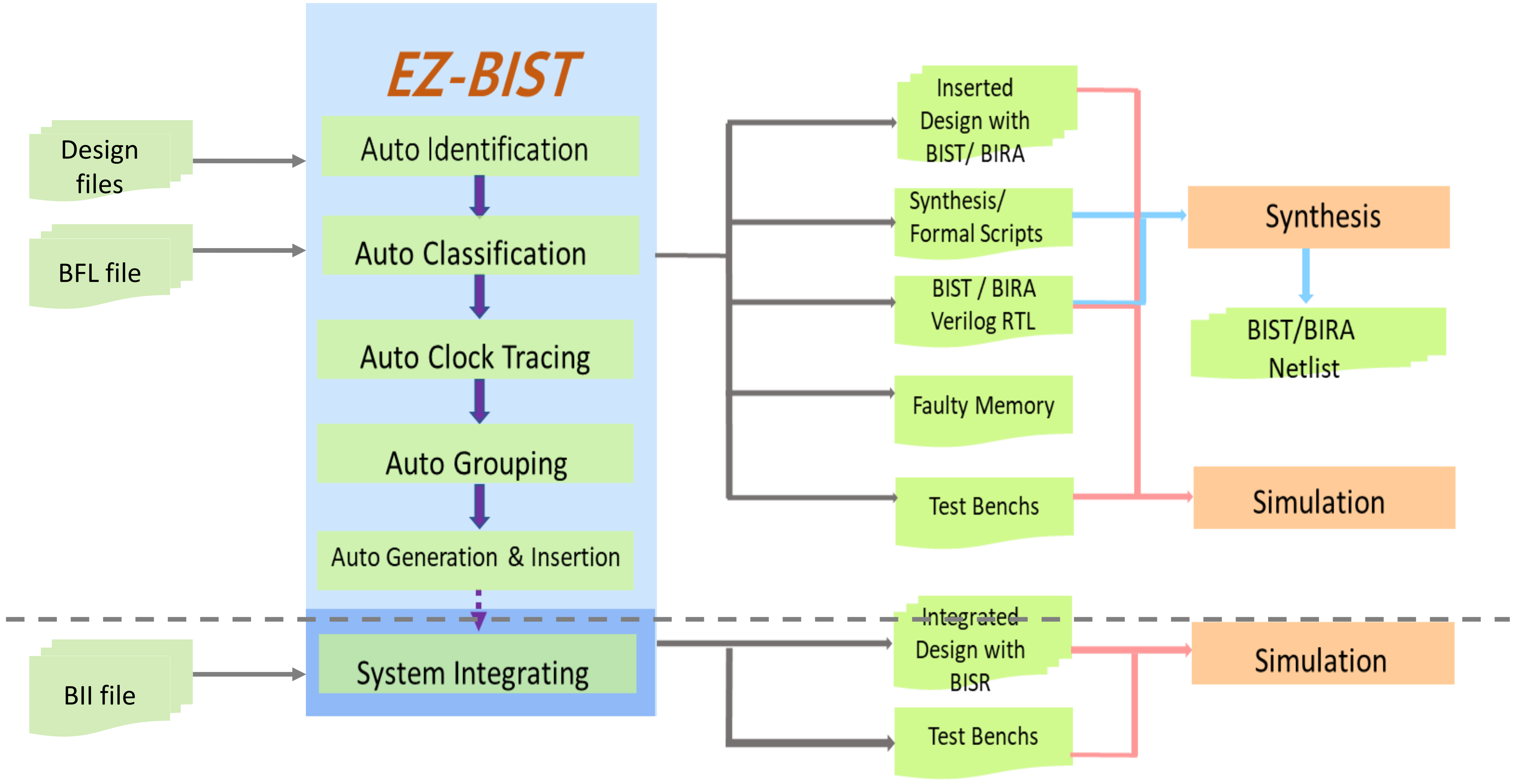
EZ-BIST Flow



**** Note:** BFL – Bist Feature List, BII – Bist Integration Information

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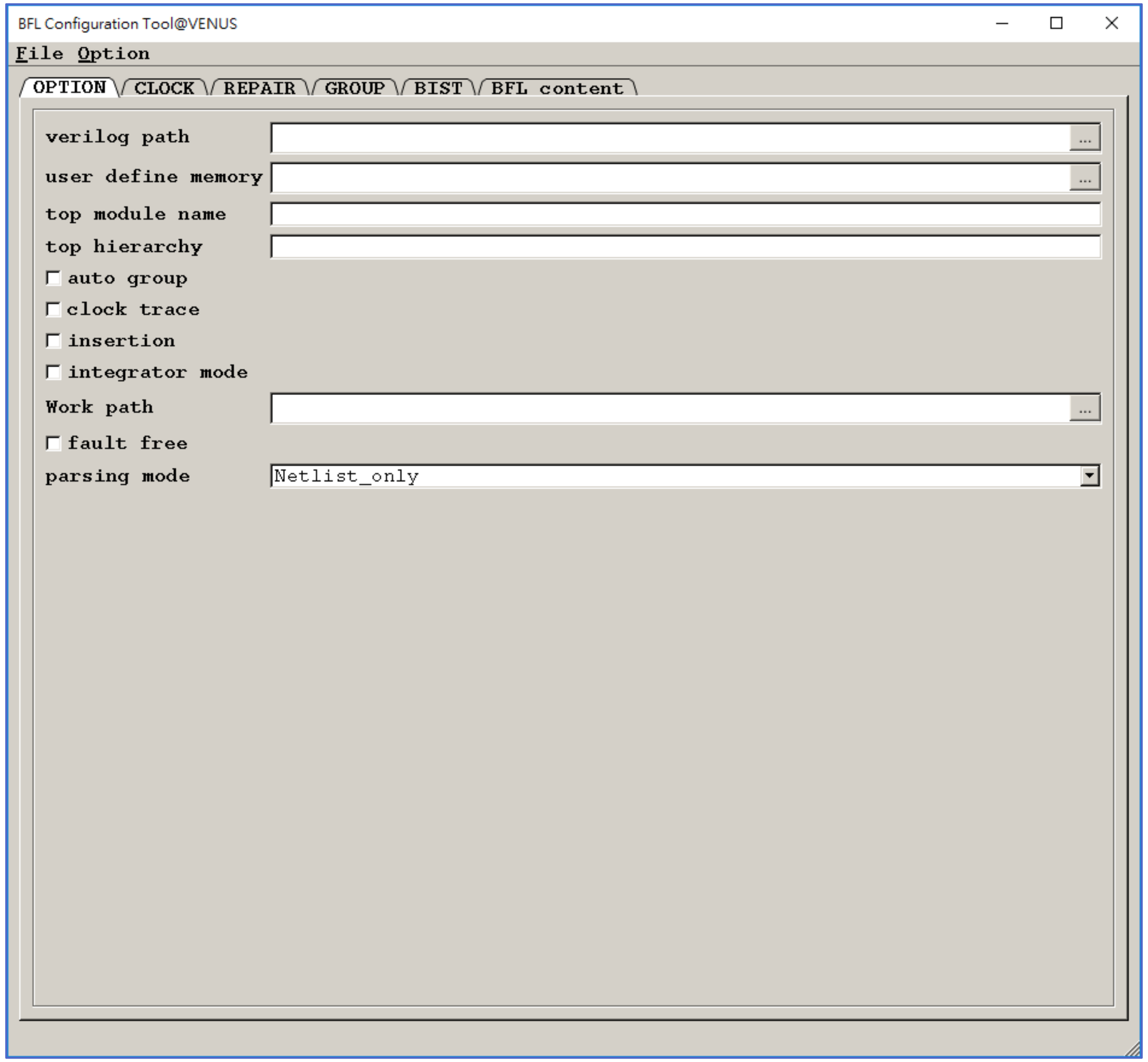
EZ-BIST GUI Interface

- ◆ Simple and interactive user interface
- ◆ Enumeration items settings
- ◆ Easy to use with clear tab orientation
- ◆ Intuitive design for users to accomplish steps easily



verilog path
user define memory
top module name
top hierarchy
☐ auto group
☐ clock trace
☐ insertion
☐ integrator mode
Work path
☐ fault free
parsing mode: Netlist_only

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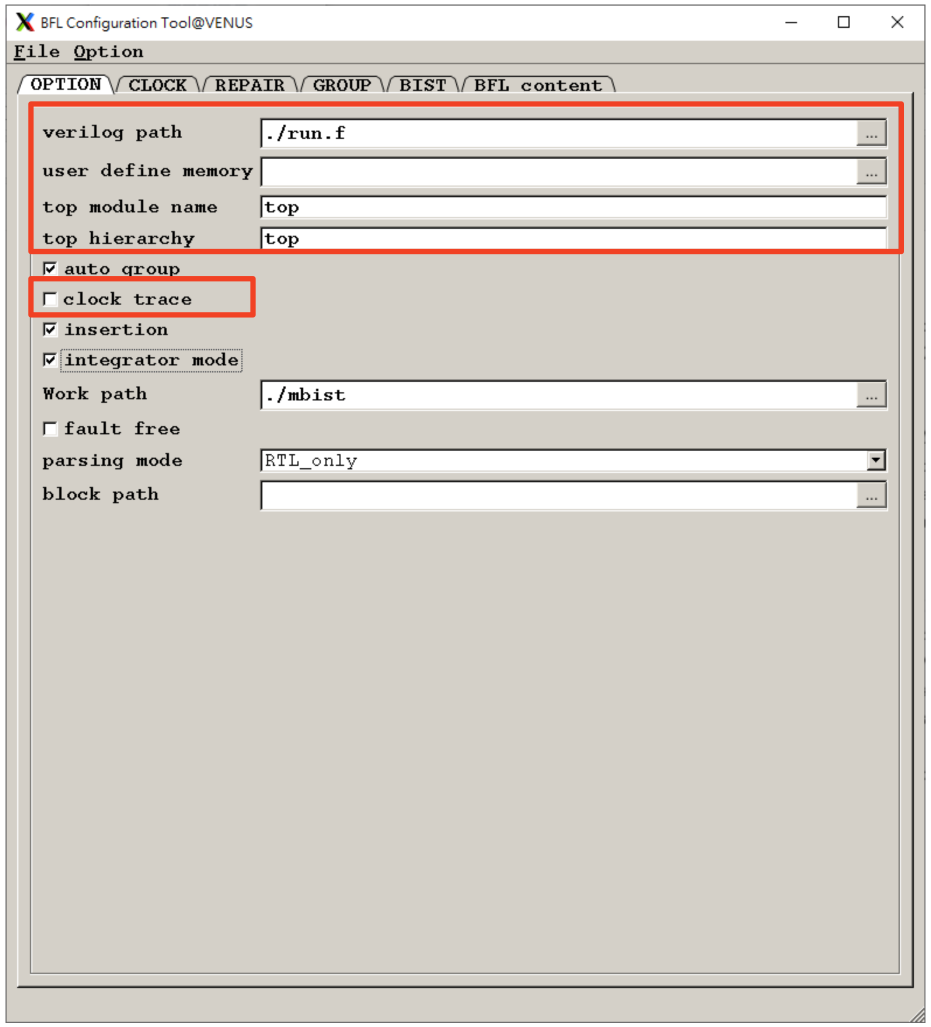
Operation Example – General Setting

- **verilog_path : ./run.f**
  - Specify Verilog file paths for EZ-BIST
- **user_define_memory** :
  - If memories does not support in EZ-BIST tool database. Users can describe these memory models according to "user defined memory" template. After that, specify these "user defined memory" filename to "user_define_memory" in BFL file
- **top_module_name : top**
  - Specify top module name of system design
- **top_hierarchy : top**
  - Specify design hierarchy which BIST circuit will be inserted
- **clock_trace : no**
  - To disable/enable auto clock tree tracing function



verilog path	./run.f
user define memory	
top module name	top
top hierarchy	top
[✓] auto group	
[ ] clock trace	
[✓] insertion	
[✓] integrator mode	
Work path	./mbist
[ ] fault free	
parsing mode	RTL_only
block path	

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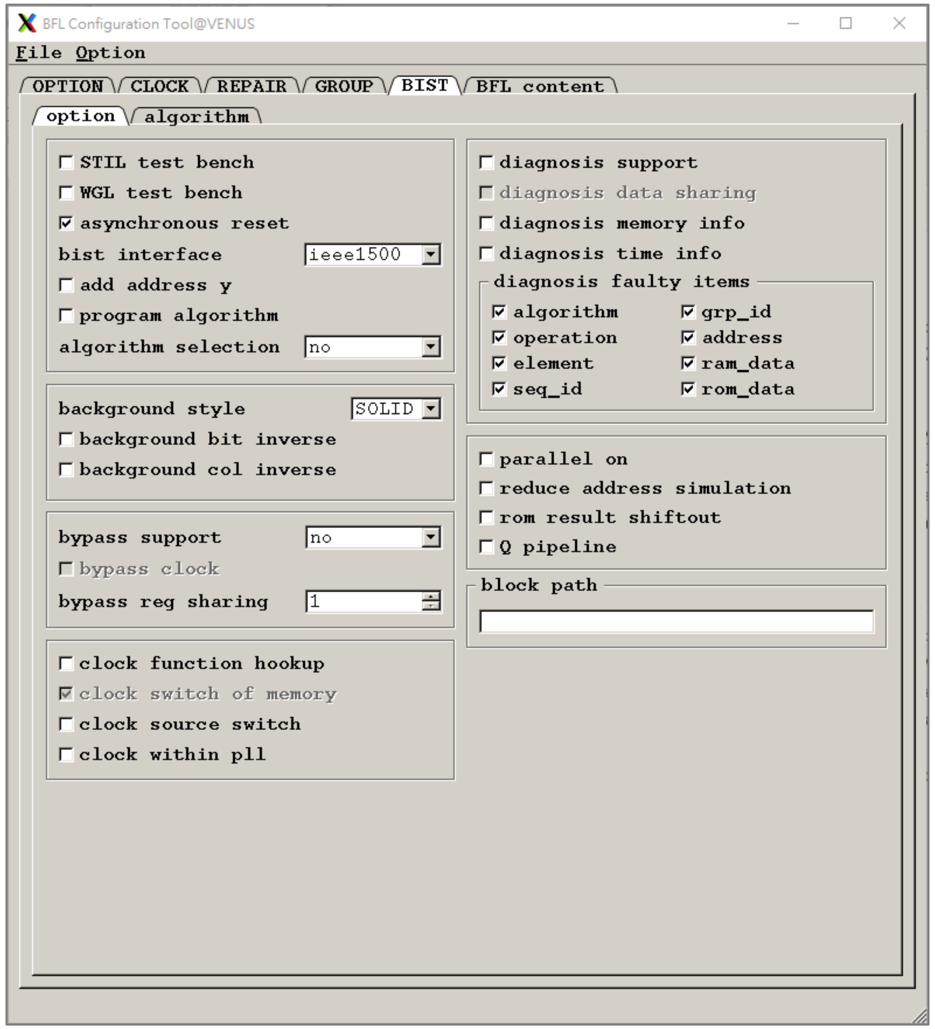
Operation Example – BIST Related Setting

- ◆**STIL_test_bench: no**
  - ■If STIL_test_bench sets yes, it will generate a test bench with STIL format
- ◆**WGL_test_bench: no**
  - ■If WGL_test_bench sets yes, it will generate a test bench with WGL (Waveform Generation Language) format
- ◆**asynchronous_reset : yes**
  - ■Specify asynchronous or synchronous reset of MBIST/BISR.
  - ■If "Yes", reset while reset signal assert
  - ■If "no", reset while rising-edge of MCK signal
- ◆**bist_interface :**
  - ■basic, minibist, IEEE 1500 and IEEE 1149.1 (JTAG)



☐ STIL test bench
☐ WGL test bench
☑ asynchronous reset
bist interface: ieee1500
☐ add address y
☐ program algorithm
algorithm selection: no

background style: SOLID
☐ background bit inverse
☐ background col inverse

bypass support: no
☐ bypass clock
bypass reg sharing: 1

☐ clock function hookup
☑ clock switch of memory
☐ clock source switch
☐ clock within pll

☐ diagnosis support
☐ diagnosis data sharing
☐ diagnosis memory info
☐ diagnosis time info

diagnosis faulty items

☑ algorithm	☑ grp_id
☑ operation	☑ address
☑ element	☑ ram_data
☑ seq_id	☑ rom_data

☐ parallel on
☐ reduce address simulation
☐ rom result shiftout
☐ Q pipeline

block path:

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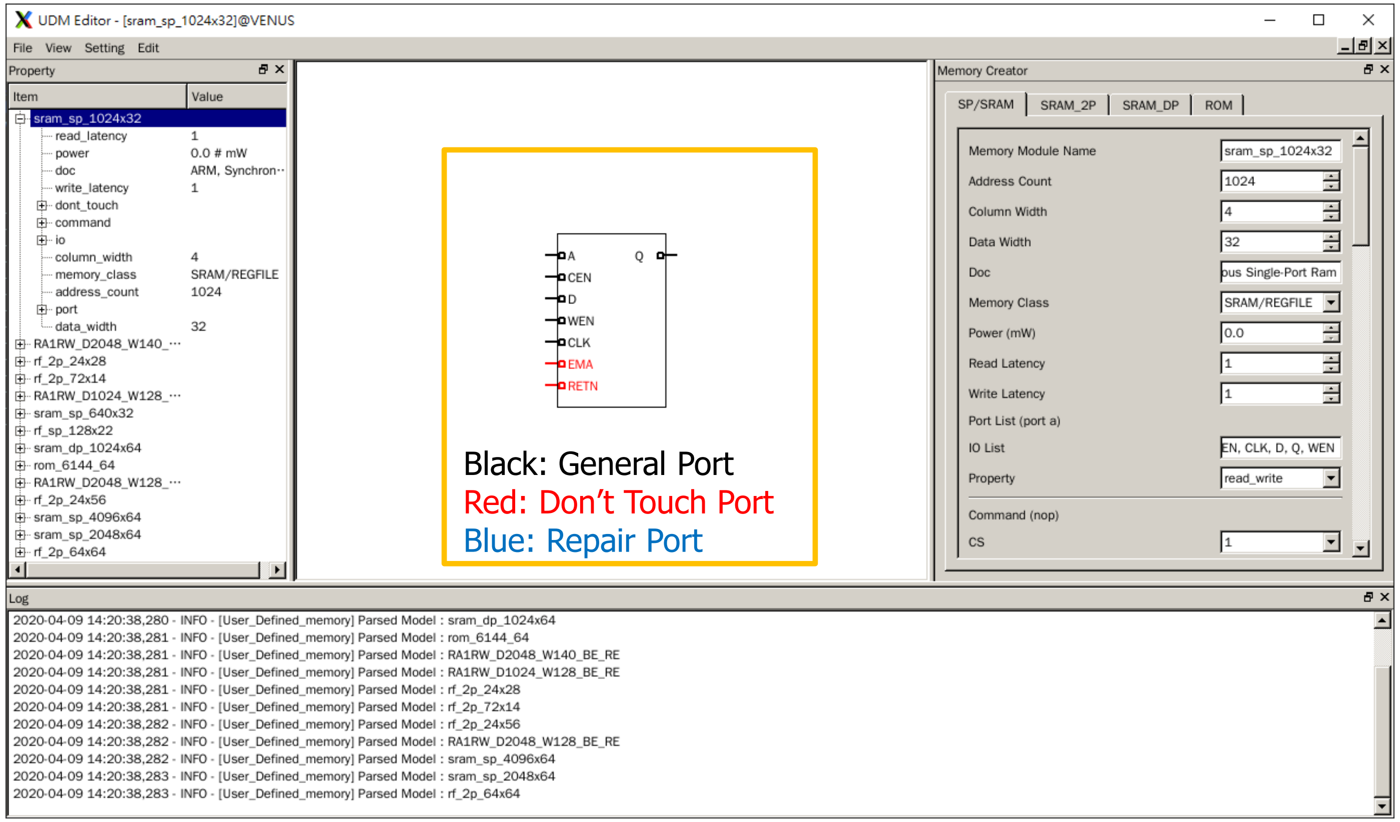
UDM – User Define Memory

- UDM offers customers adding their own memory model
- GUI interface operation
- Supports Single port, 2 ports, dual port SRAM and ROM



Item	Value
sram_sp_1024x32	
read_latency	1
power	0.0 # mW
doc	ARM, Synchron··
write_latency	1
dont_touch	
command	
io	
column_width	4
memory_class	SRAM/REGFILE
address_count	1024
port	
data_width	32
RA1RW_D2048_W140_···	
rf_2p_24x28	
rf_2p_72x14	
RA1RW_D1024_W128_···	
sram_sp_640x32	
rf_sp_128x22	
sram_dp_1024x64	
rom_6144_64	
RA1RW_D2048_W128_···	
rf_2p_24x56	
sram_sp_4096x64	
sram_sp_2048x64	
rf_2p_64x64	

Black: General Port
Red: Don't Touch Port
Blue: Repair Port

Memory Module Name	sram_sp_1024x32
Address Count	1024
Column Width	4
Data Width	32
Doc	ous Single-Port Ram
Memory Class	SRAM/REGFILE
Power (mW)	0.0
Read Latency	1
Write Latency	1
Port List (port a)	
IO List	EN, CLK, D, Q, WEN
Property	read_write
Command (nop)	
CS	1

```
2020-04-09 14:20:38,280 - INFO - [User_Defined_memory] Parsed Model : sram_dp_1024x64
2020-04-09 14:20:38,281 - INFO - [User_Defined_memory] Parsed Model : rom_6144_64
2020-04-09 14:20:38,281 - INFO - [User_Defined_memory] Parsed Model : RA1RW_D2048_W140_BE_RE
2020-04-09 14:20:38,281 - INFO - [User_Defined_memory] Parsed Model : RA1RW_D1024_W128_BE_RE
2020-04-09 14:20:38,281 - INFO - [User_Defined_memory] Parsed Model : rf_2p_24x28
2020-04-09 14:20:38,281 - INFO - [User_Defined_memory] Parsed Model : rf_2p_72x14
2020-04-09 14:20:38,282 - INFO - [User_Defined_memory] Parsed Model : rf_2p_24x56
2020-04-09 14:20:38,282 - INFO - [User_Defined_memory] Parsed Model : RA1RW_D2048_W128_BE_RE
2020-04-09 14:20:38,282 - INFO - [User_Defined_memory] Parsed Model : sram_sp_4096x64
2020-04-09 14:20:38,283 - INFO - [User_Defined_memory] Parsed Model : sram_sp_2048x64
2020-04-09 14:20:38,283 - INFO - [User_Defined_memory] Parsed Model : rf_2p_64x64
```

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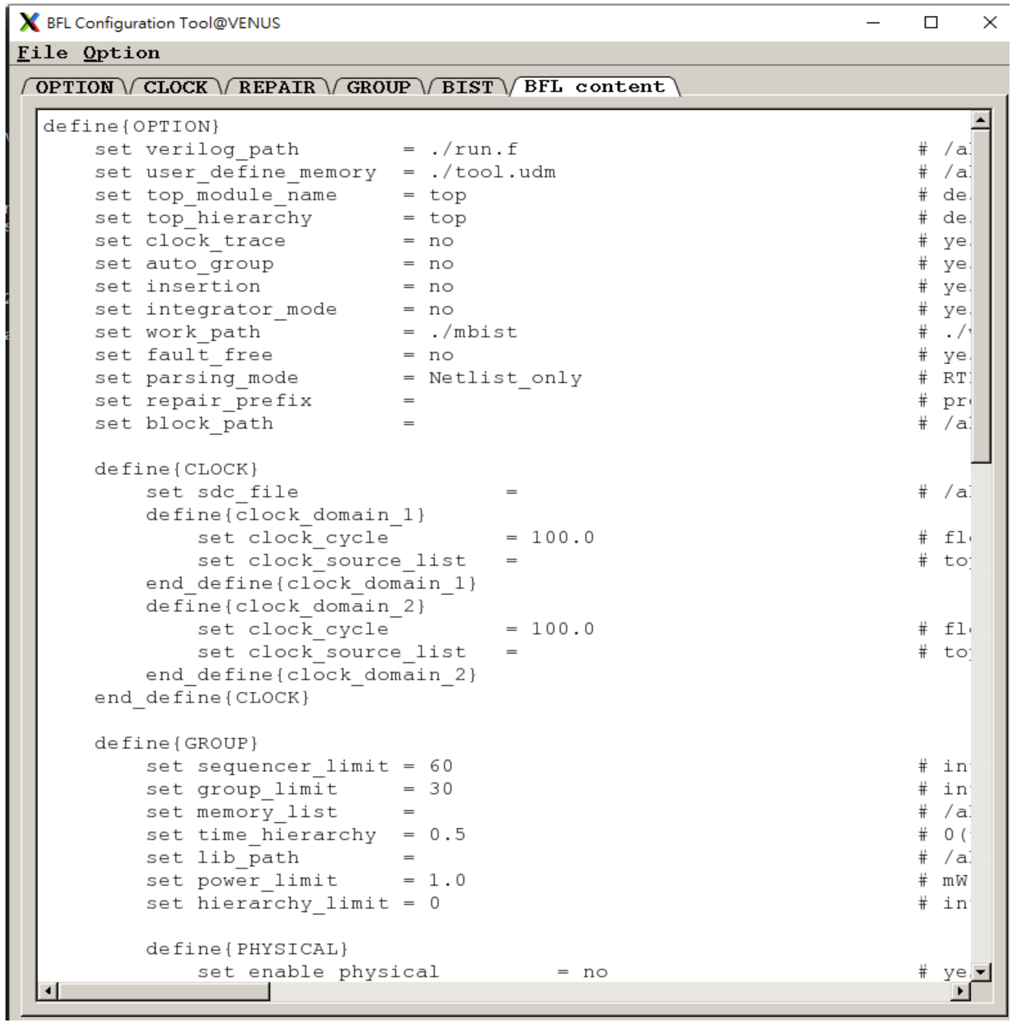
Executing BFL in EZ-BIST

- ◆Insert BIST circuit into cusomers design
- ◆ One click [File] -> [Run] to perform BIST processing
- ◆ The same as command Line Interface as following
  - ■ $ start -bfl start_template.bfl



```
define{OPTION}
    set verilog_path          = ./run.f                                     # /a
    set user_define_memory    = ./tool.udm                                  # /a
    set top_module_name       = top                                         # de
    set top_hierarchy         = top                                         # de
    set clock_trace           = no                                          # ye
    set auto_group            = no                                          # ye
    set insertion             = no                                          # ye
    set integrator_mode       = no                                          # ye
    set work_path             = ./mbist                                     # ./
    set fault_free            = no                                          # ye
    set parsing_mode          = Netlist_only                                # RT
    set repair_prefix         =                                             # pr
    set block_path            =                                             # /a

    define{CLOCK}
        set sdc_file                  =                                     # /a
        define{clock_domain_1}
            set clock_cycle           = 100.0                               # fl
            set clock_source_list     =                                     # to
        end_define{clock_domain_1}
        define{clock_domain_2}
            set clock_cycle           = 100.0                               # fl
            set clock_source_list     =                                     # to
        end_define{clock_domain_2}
    end_define{CLOCK}

    define{GROUP}
        set sequencer_limit = 60                                            # in
        set group_limit     = 30                                            # in
        set memory_list     =                                               # /a
        set time_hierarchy  = 0.5                                           # 0(
        set lib_path        =                                               # /a
        set power_limit     = 1.0                                           # mW
        set hierarchy_limit = 0                                             # in

        define{PHYSICAL}
            set enable_physical          = no                               # ye
```

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Thank You

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