iSTART
iSTART-TEK INC.

A Non-volatile Memory Platform You've Never Seen

Project Leader Engineer

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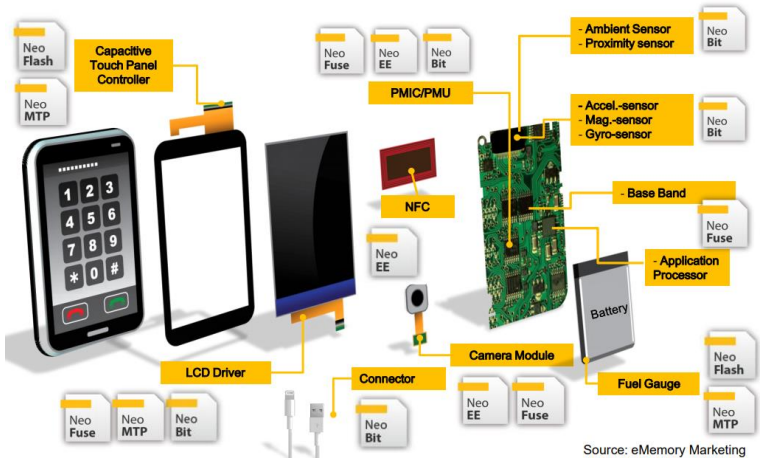
精彩回顧：**https://youtu.be/V2FDaxBDYWg**

Outline

- NVM Platform Application
- NVM Platform Function
- Summary

NVM Platform Application

NVM Platform Can Support Different NVMs

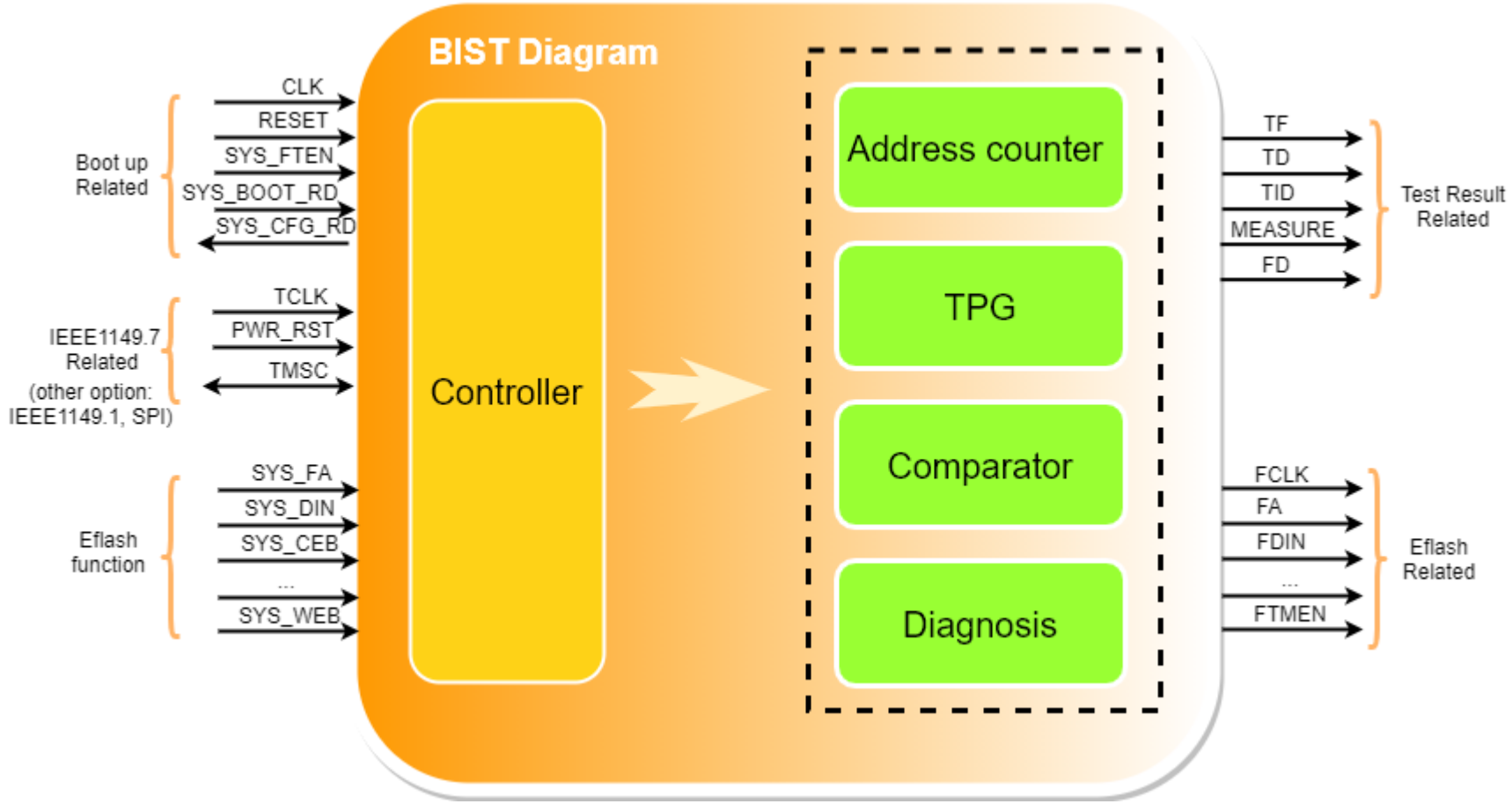


Sources : Association Française des Diabétiques et Fédération Française des Diabétiques

source:tsmc

NVM Platform Function

NVM Platform - BIST Diagram



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NVM Platform - Support Foundry

- ◆eFlash series
- ◆MTP series
- ◆MRAM , RRAM series

NVM Platform - Generate Different Clock

- According to the various clock frequencies on the chip design, NVM Platform can generate the time parameters in a short time. Engineers can get various optimized parameters according to the condition of various status anytime.

NVM Platform - Support Different Test Items

- ◆Fully customized test items
- ◆Part of the test items (Options)
- ◆Flash test algorithm (March FT)

March FT	GPD	GED	DPD	DED	OE	RD
	100%	100%	100%	100%	100%	100%
	SAF	TF	SOF	AF	CFst	
	100%	100%	100%	100%	100%	

NVM Platform - Support Different Communication Interfaces

- **Users can choose one of the following three methods:**
  - IEEE1149.1 interface (5 ports)
  - IEEE1149.7 interface (3 ports)
  - SPI interface

NVM Platform - Support Different Pattern Vector Format

◆STIL vector

Example

```
Pattern example {
        W _default_WFT_;
        LABEL:    V { ALL = 00000000 00000000 00000000 00000000; }
                  V { ALL = 11111111 11111111 11111111 11111111; }
        Loop 10 {           // implemented as a multi-vector loop
                  V { ALL = 11111111 11111111 11111111 11111111; }
                  V { ALL = HHHHHHHH HHHHHHHH HHHHHHHH HHHHHHHH; }
                  V { ALL = 00000000 00000000 00000000 00000000; }
                  V { ALL = LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL; }
        }
        Loop 5 {                                  // implemented as a repeat vector
                  V { ALL = 11111111 11111111 11111111 11111111; }
        }
        Stop;
}
```

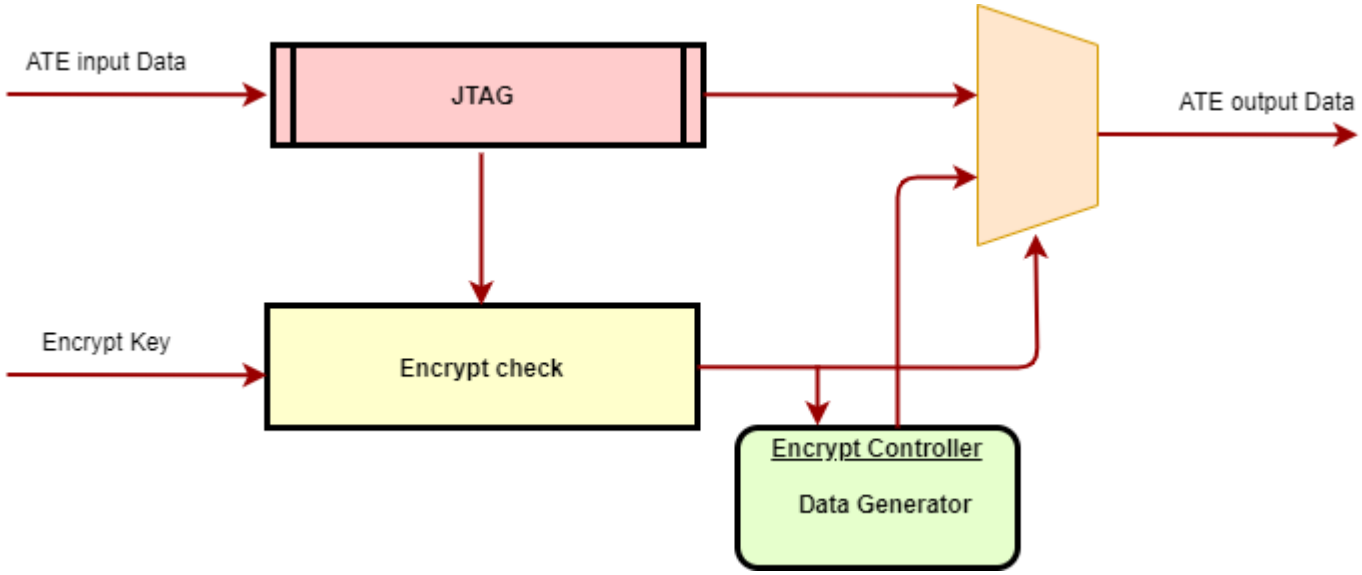
◆TEXT vector (For different ATE)

- Example : CHROMA, J750 , V93K... etc

NVM Platform - Security Protect

- Security and testability are the important factors affecting designing for testability.
- Support a secure method to protect data of the JTAG interface. The encrypt key has 128 bits .

NVM Platform - Security Diagram



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Summary

The Platform NVM IP of IoT Applications

The technology improvement

- With faster wireless networks, superior sensors and revolution computing capabilities, the IoT improves the current devices in power, precision, and availability. It has been growing huge business opportunities.

The Platform NVM IP of IoT cases

- Wearables
- Smart Home Applications
- Health care
- Smart Cities
- Agriculture
- Industrial Automation

What iSTART Platform Offers (1)

Customized design

- Provide a customized design BIST/BISR IP functions, which can be matched with different NVM sizes to generate corresponding test/repair IP

Experience

- Many SST/ISSI eFlash BIST/BISR IP mass production experience

Flexible

- Flexible interface configuration (5 ports IEEE1149.1、3 ports IEEE 1149.7、SPI mode、customize design)

What iSTART Platform Offers (2)

Repair function

- Repair function improves the yield, and can be matched with power-on or dynamic test functions to meet the high reliability requirements of automotive and industrial grades

Easily achieve

- Customer can easily achieve a balance between test coverage and testing cost time in flexible enabled and disabled test items.

Flexible

- Perform flexible user command test actions

What iSTART Platform Offers (3)

Diagnostic

- Provide diagnostic information to determine the type and location of the error for test time optimization

Area

- Optimize the BIST/BISR area according to customer needs and support programming trimming data

Security

- Customized security design to protect the customer data safety

iSTART eFlash BIST/BISR IP Advantages

Silicon Proven

eFlash BIST and BISR IP repeated orders, the only eFlash BIST and BISR IP partner

110nm, 55nm, 40nm silicon verification experience

BIST and BISR IP shipped to Japanese automotive IC manufacturers

Tool Platform advantages

Automation

- Directly generate corresponding BIST/BISR IP for different NVM size in GUI tool platform based
- Simple platform, good reusability, greatly reducing NVM BIST design coding time
- Testbench directly generates the corresponding ATE test vector STIL/Text format

Flexible

- Support NVM Scramble test design
- Output BIST design is Soft IP, easily integrate into SoC design

Diagnosis function

- Customer feedback test time is shortened to 1/5 of original test time, greatly reducing test cost

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