iSTART
iSTART-TEK INC.

Customized Cases

Technical Support Department
TP Hsieh

精彩回顧：**https://youtu.be/9DPdRJF8nD0**

iSTART

Outline

- Europe S-company
- Korea A-company
- China Q-company
- Taiwan F-company

S-company / France

iSTART

Background

- ◆Europe's third-largest fabless semiconductor company
- ◆Products are advanced LTE , 4G, 5G chips and IoT module
- ◆Request professional and high-quality memory testing and repairing technology
- ◆ Sign a new agreement to extend the collaboration relationship

Customer Request Function

- Usually we run BIST with all power domains ON when we have IRdrop issue (too many memories running at the same time) we disable some controller and run BIST in 2 steps.
- For the Repair, it’s run when system reset is active. After each power down we re-pulse the reset and launch repair procedure to shift-in the repair signature.
- We do need sometimes to place a controller in dedicated hierarchy.

Customized Function - Controller Hierarchy Specific

- **Low power design methodology**
  - Arrange controller of BIST in dedicated level of SoC
    - To satisfy with arrangement of power domain and clock domain of SoC
    - Users can save power consumption by setting controller of BIST in dedicated power domain
- **INTEG/BISR/RP CTR/BIST CTR could be assign to specific hierarchy**
- **In BFL file, 2 parameters need to set**
  - top_module_name
  - top_hierarchy
- **In BII file, 2 parameters need to set**
  - top_module_name
  - TAP_hierarhy

A-company / Korea

iSTART

Background

- A fabless and leading provider in ASIC industry
- Focusing on the 4th industry ASIC such as AI, 5G, Block-Chain, and IoT to lead the market
- TSMC Value Chain Aggregator (VCA)
- ARM Approved Design Partner (ADP)
- Project memory instances up to 3000
- Need a stronger and efficiency tool to fulfill MBIST and MBISR circuit design

Customer Request Function

- I want SDC file, that is automatically generated from START tool, with full hierarchy including mapping points and dedicate ports of the clocks and other BIST signals at BII mode.
- Also, I want to run post STA at BIST mode using the SDC file.
- I have memories without scan-function and memories with scan-function. I would like to apply the bypass option to memories without scan-function for SCAN and apply no-bypass option to memories with scan-function.

Customized Function

- ◆iSTART provide a new tool to merge all TCL files to a single TCL file. This single merged TCL file will include all hierarchy paths information. A-company can use this merged TCL file to compile and generate the SDC file required.
- ◆iSTART tool will add a scan keyword judgment to decide applying bypass option to memories without scan-function for SCAN and applying no-bypass option to memories with scan-function.

Q-company / China

iSTART

Background

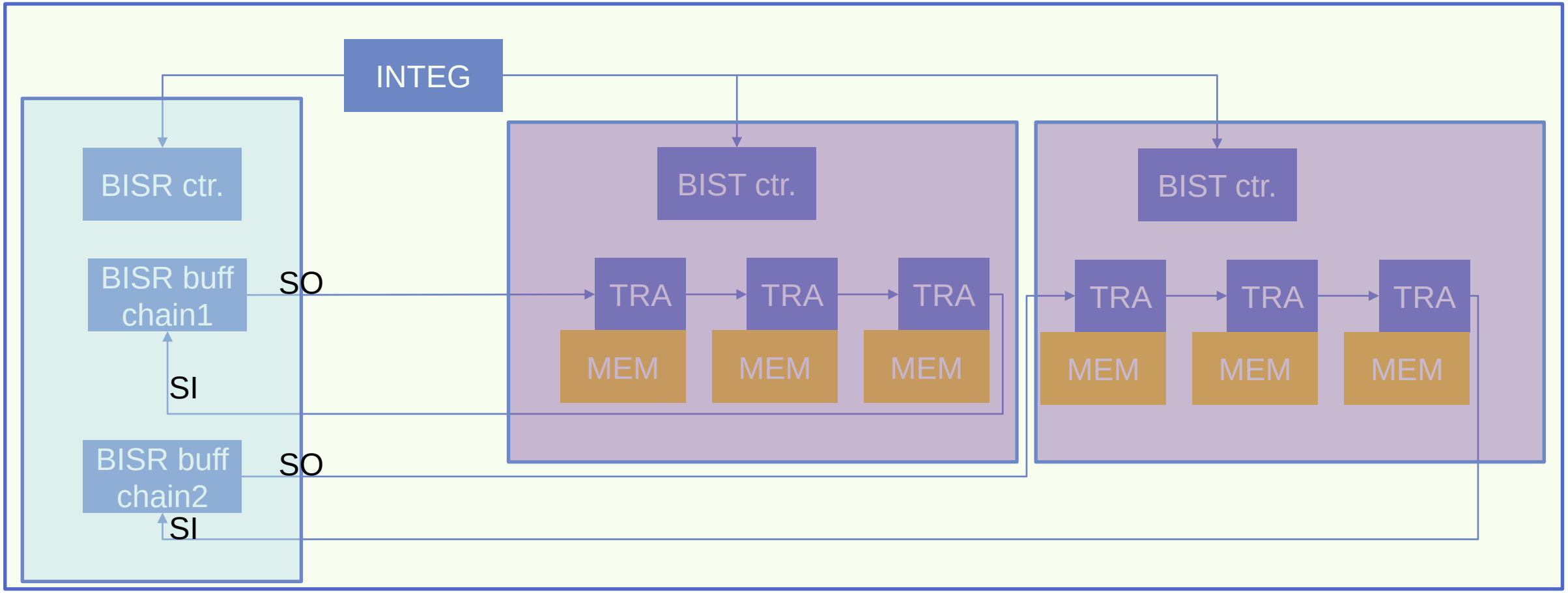
- Design service company in Wuxi Jiangsu, China
- Large and complex AI chip project
- Technology node 28 nm
- Project uses 8 CPUs and 4 GPUs
- Memory instances exceed 2000
- Need an efficient tool to finish BIST & BISR design in a short time

Customer Request Function

◆Require multi-chain TRA repair design to save power consumption.

Customized Function – Multi-Chain

◆**Designers can arrange chain to satisfy with requirement of SoC's low power by using Multi-Chain.**



iSTART

F-comany / Taiwan

iSTART

Background

- Develop human interface related technology
- Products has touch IC, pressure sensor IC, TFT LCD/OLED driver IC, in-cell display touch single chip (IDC/TDDI), capacitive fingerprint recognition IC, optical fingerprint….

Customer Request Function

- **This company needs a particular testing method to test their memory. They hope that tool supports a function to let designer define testing algorithm by themselves.**

Customer Request Function – Program Algorithm

◆**Designers can self-define elements in BFL file**

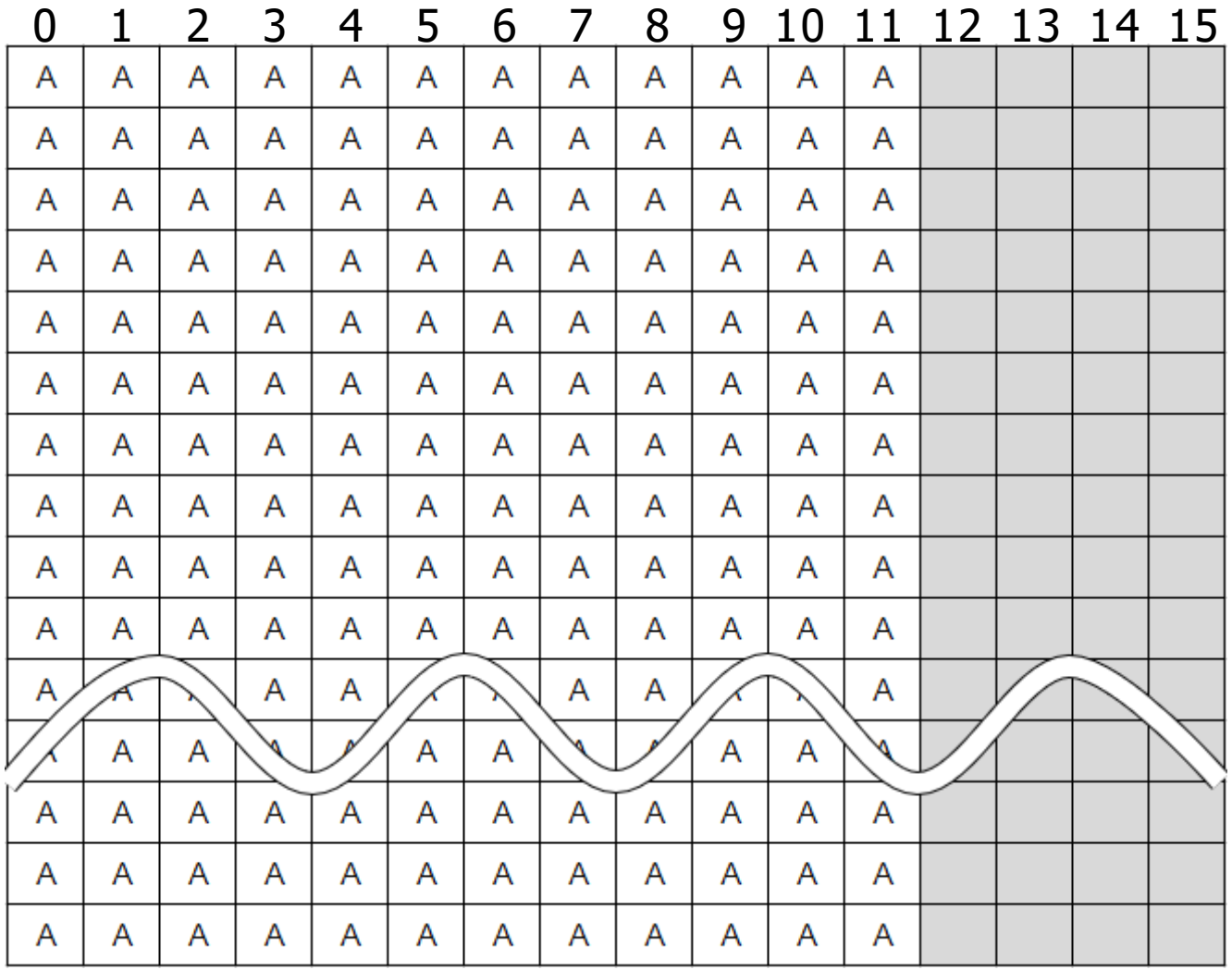
Algorithm	Description
MATS	$\{ \Updownarrow (w0); \Updownarrow (r0, w1); \Updownarrow (r1) \}$
MATS+	$\{ \Updownarrow (w0); \Uparrow (r0, w1); \Downarrow (r1, w0) \}$
MATS++	$\{ \Updownarrow (w0); \Uparrow (r0, w1); \Downarrow (r1, w0, r0) \}$
MARCH X	$\{ \Updownarrow (w0); \Uparrow (r0, w1); \Downarrow (r1, w0); \Updownarrow (r0) \}$
MARCH C–	$\{ \Updownarrow (w0); \Uparrow (r0, w1); \Uparrow (r1, w0); \Downarrow (r0, w1); \Downarrow (r1, w0); \Updownarrow (r0) \}$
MARCH A	$\{ \Updownarrow (w0); \Uparrow (r0, w1, w0, w1); \Uparrow (r1, w0, w1); \Downarrow (r1, w0, w1, w0); \Downarrow (r0, w1, w0) \}$
MARCH Y	$\{ \Updownarrow (w0); \Uparrow (r0, w1, r1); \Downarrow (r1, w0, r0); \Updownarrow (r0) \}$
MARCH B	$\{ \Updownarrow (w0); \Uparrow (r0, w1, r1, w0, r0, w1); \Uparrow (r1, w0, w1); \Downarrow (r1, w0, w1, w0); \Downarrow (r0, w1, w0) \}$

```
define{algorithm}
    set single_port       = Mar
    set two_port          = Mar
    set dual_port         = Mar
end_define{algorithm}

define{algorithm_programmable}
    set support_elements      = wa, rawbwawb, rbwawb
    set max_prog_element      = 6              # integer bigger than 0
end_define{algorithm_programmable}
```

Customer Request Function - Particular Testing Method

◆By using ADR_INC setting, memory testing can skip specified address and jump to next memory row to do testing



iSTART

芯测科技